FIG. 1

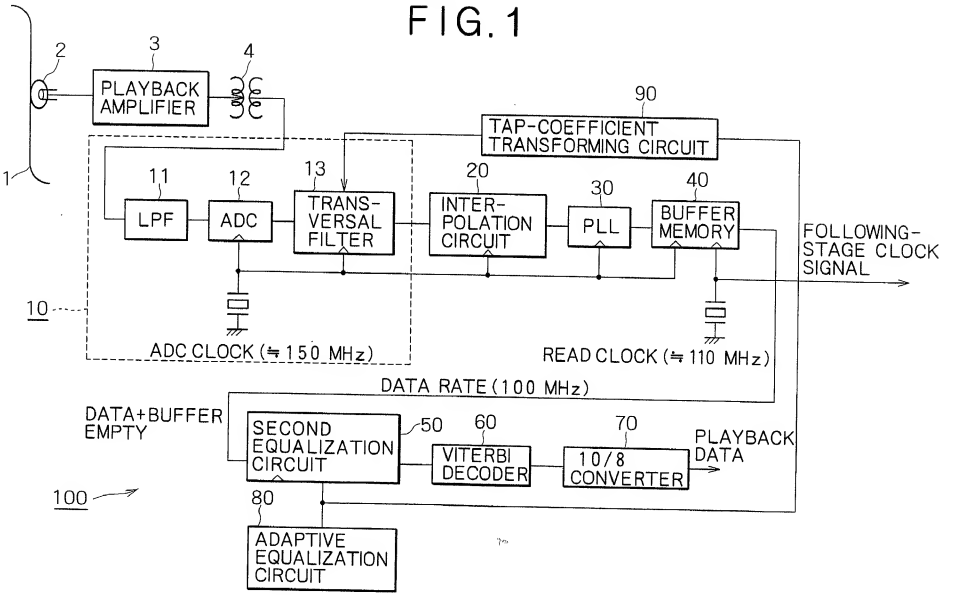

1
2
3
PLAYBACK AMPLIFIER
4
90
TAP-COEFFICIENT TRANSFORMING CIRCUIT
11
LPF
12
ADC
13
TRANS-VERSAL FILTER
20
INTER-POLATION CIRCUIT
30
PLL
40
BUFFER MEMORY
FOLLOWING-STAGE CLOCK SIGNAL
10
ADC CLOCK (≒150 MHz)
READ CLOCK (≒110 MHz)
DATA RATE (100 MHz)
DATA+BUFFER EMPTY
SECOND EQUALIZATION CIRCUIT
50
60
VITERBI DECODER
70
10/8 CONVERTER
PLAYBACK DATA
100
80
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 2

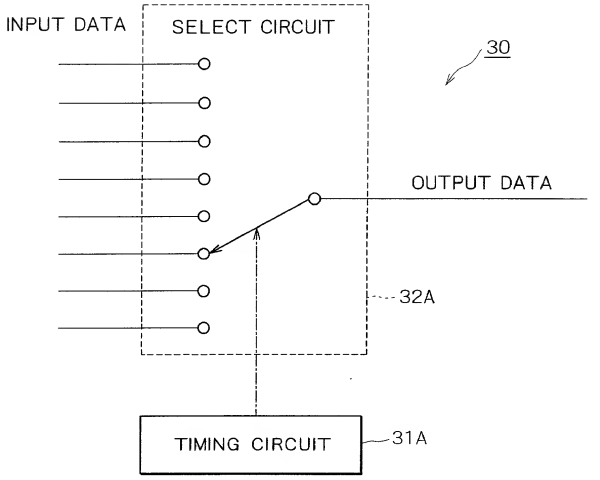


FIG. 3

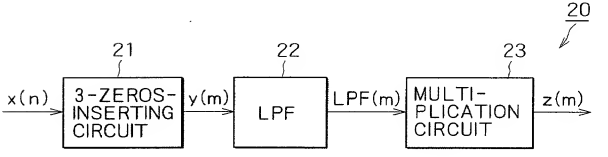


FIG. 4A

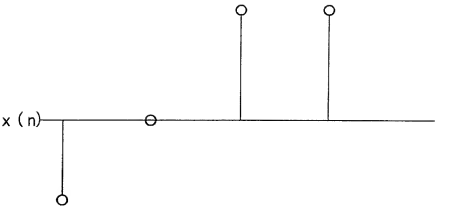


FIG. 4B

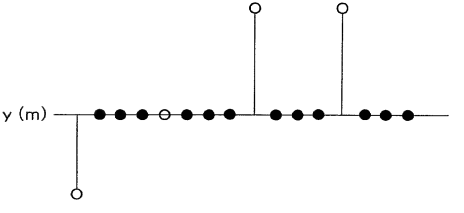


FIG. 4C

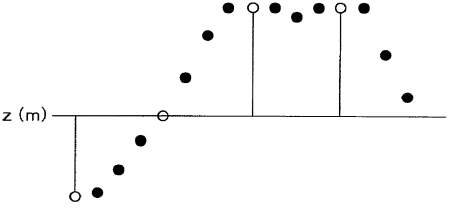


FIG. 5

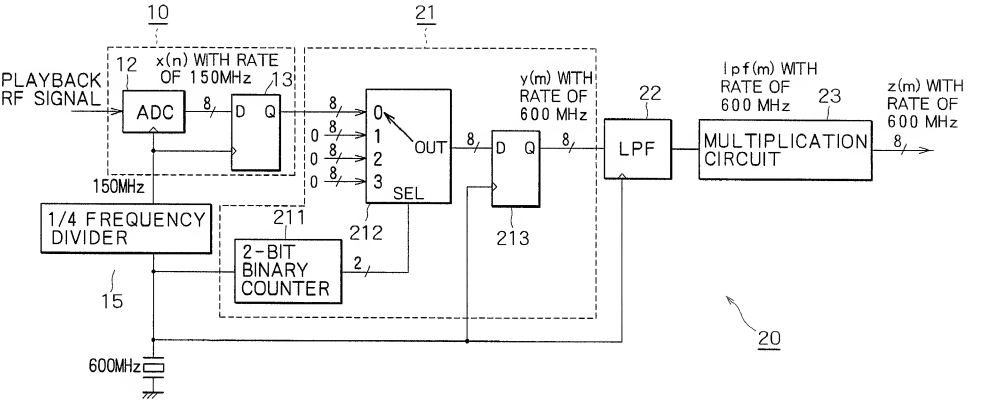

10
21
PLAYBACK RF SIGNAL
12
x(n) WITH RATE OF 150MHz
13
ADC
8
D Q
0
1
2
3
OUT
SEL
y(m) WITH RATE OF 600 MHz
22
lpf(m) WITH RATE OF 600 MHz
23
z(m) WITH RATE OF 600 MHz
LPF
MULTIPLICATION CIRCUIT
150MHz
1/4 FREQUENCY DIVIDER
211
212
213
2-BIT BINARY COUNTER
2
15
600MHz
20

FIG.6

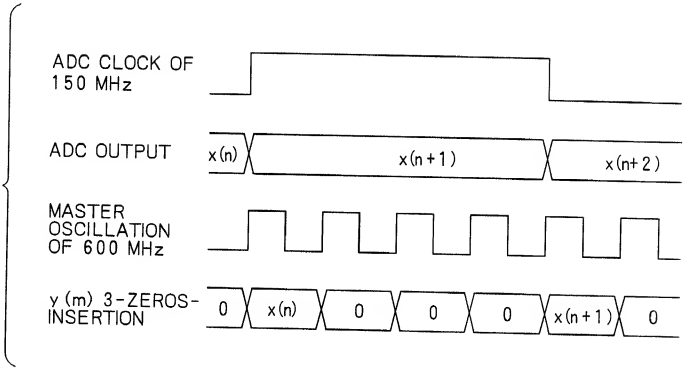

ADC CLOCK OF 150 MHz
ADC OUTPUT
x(n)
x(n+1)
x(n+2)
MASTER OSCILLATION OF 600 MHz
y(m) 3-ZEROS-INSERTION
0
x(n)
0
0
0
x(n+1)
0

FIG. 7A

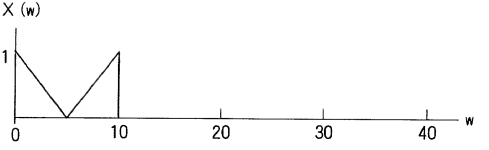


FIG. 7B

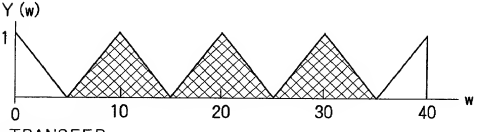


FIG. 7C

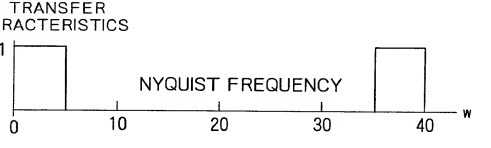


FIG. 7D

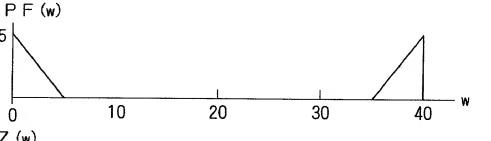


FIG. 7E

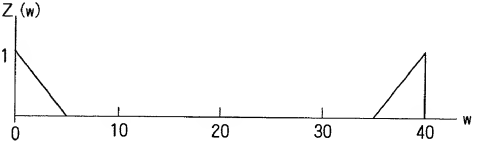


FIG. 8

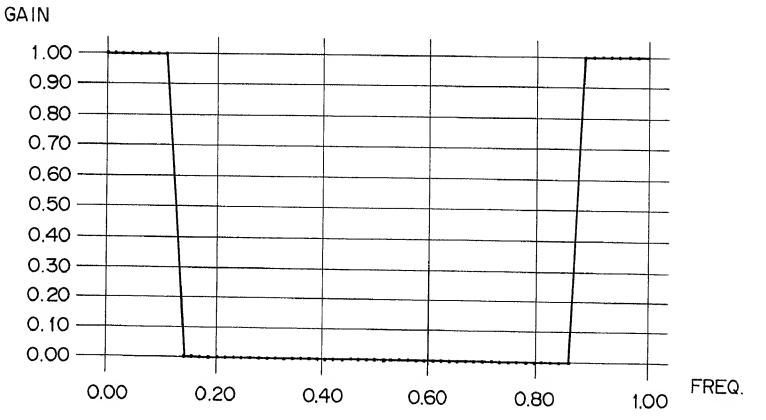

TRANSFER CHARACTERISTICS OF THE x4 INTERPOLATION LPF
GAIN
1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
0.00
0.20
0.40
0.60
0.80
1.00
FREQ.

FIG. 9

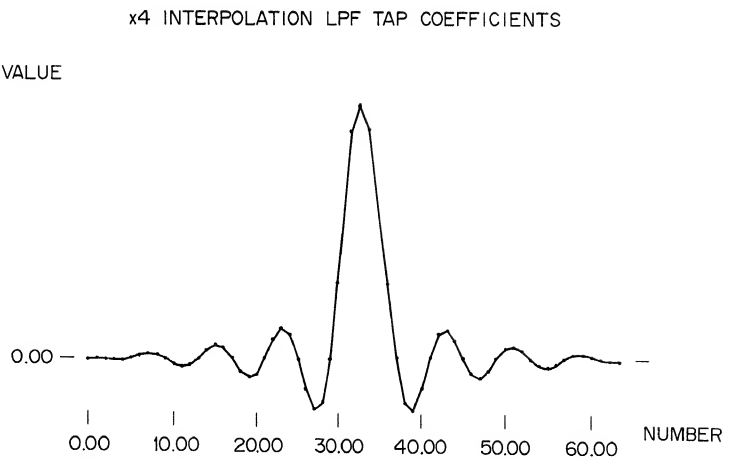


FIG. 10A

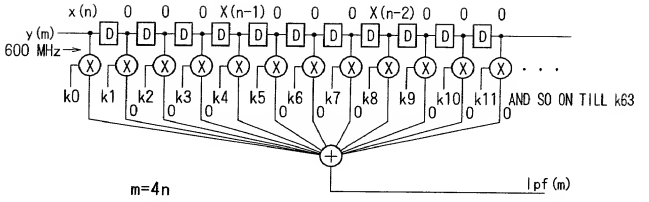


FIG. 10B

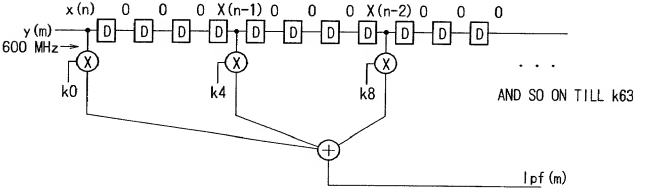


FIG. 10C

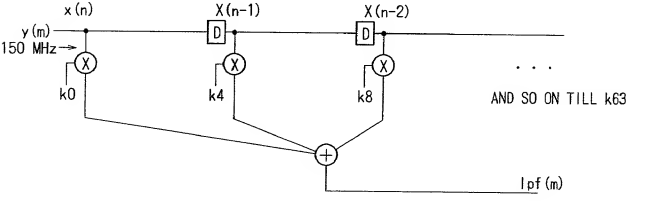


FIG. 11A

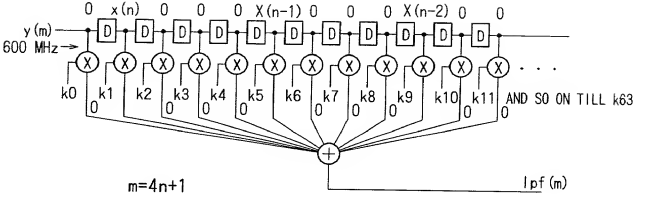


FIG. 11B

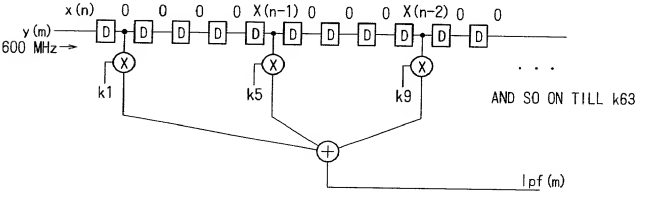


FIG. 11C

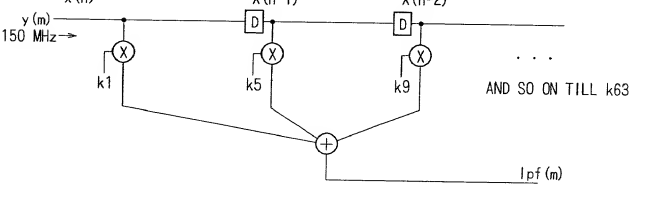


FIG. 12A

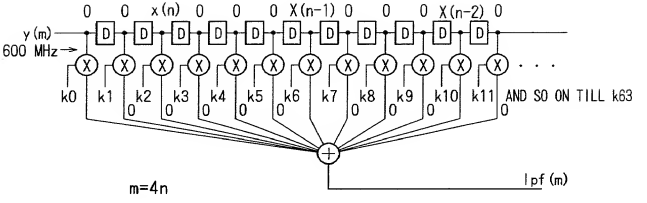


FIG. 12B

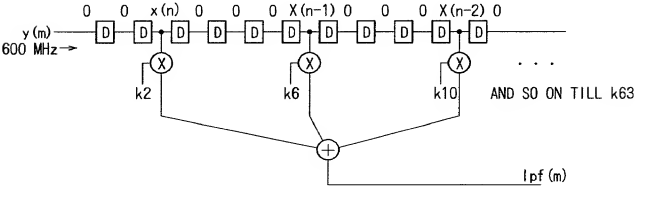


FIG. 12C

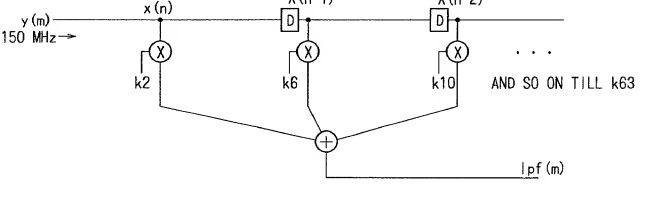


FIG. 13A

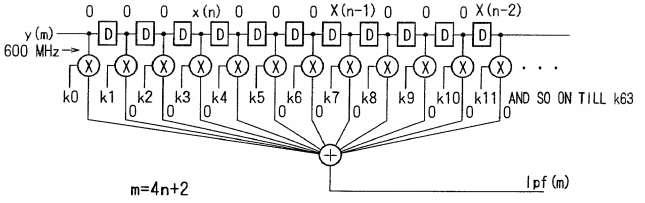


FIG. 13B

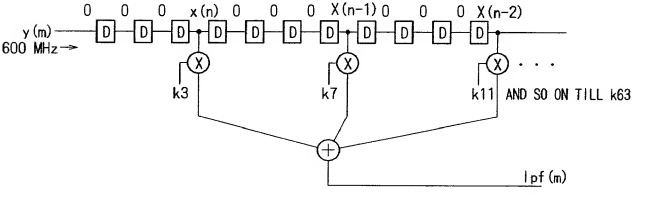


FIG. 13C

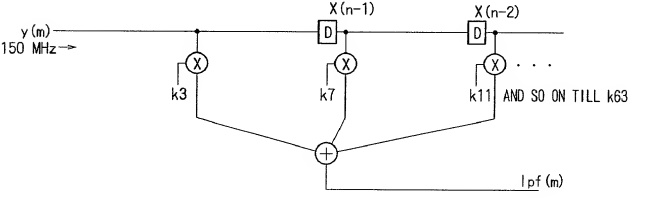


FIG. 14

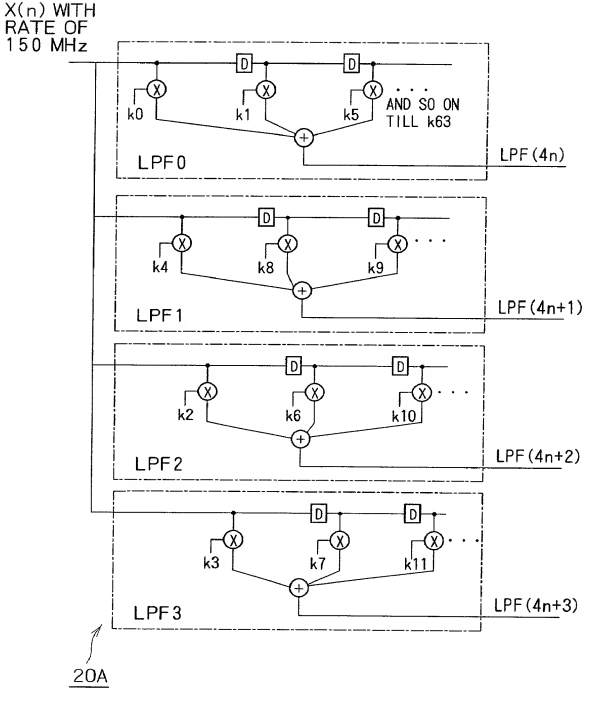

X(n) WITH
RATE OF
150 MHz
D
D
D
X
X
X
k0
k1
k5
AND SO ON
TILL k63
LPF0
LPF(4n)
k4
k8
k9
LPF1
LPF(4n+1)
k2
k6
k10
LPF2
LPF(4n+2)
k3
k7
k11
LPF3
LPF(4n+3)
+
20A

FIG. 15

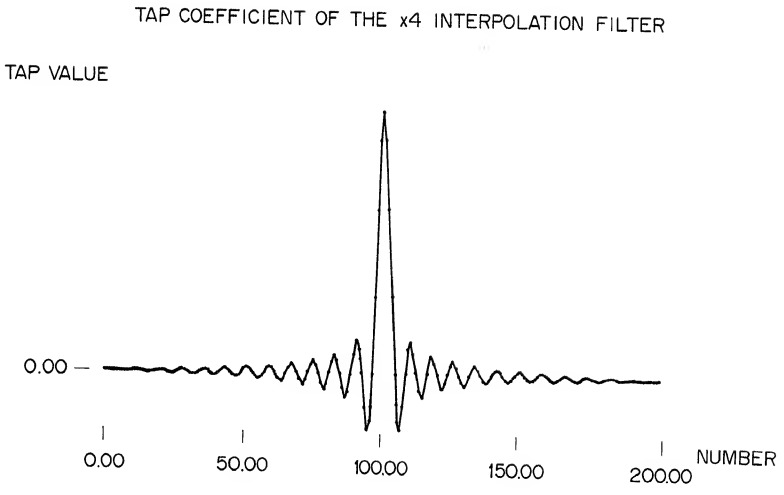

TAP COEFFICIENT OF THE x4 INTERPOLATION FILTER
TAP VALUE
0.00
0.00
50.00
100.00
150.00
200.00
NUMBER

FIG. 16

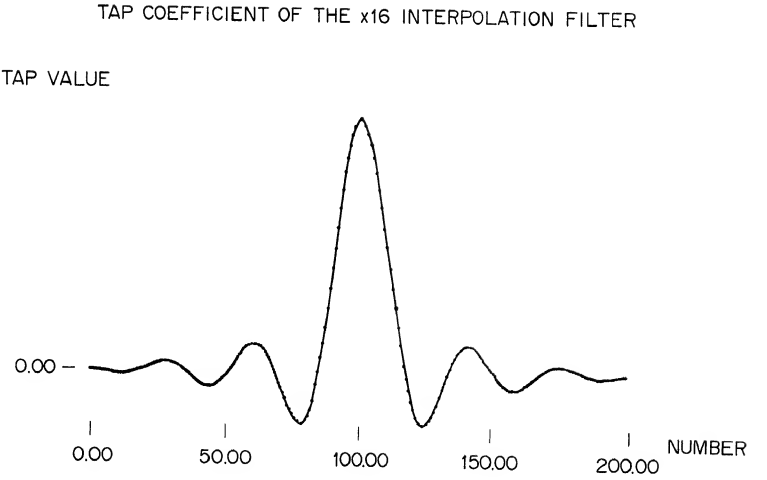


FIG. 17

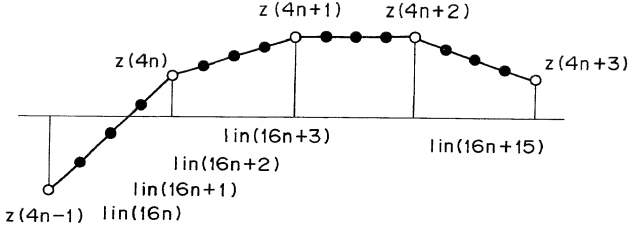


FIG. 18

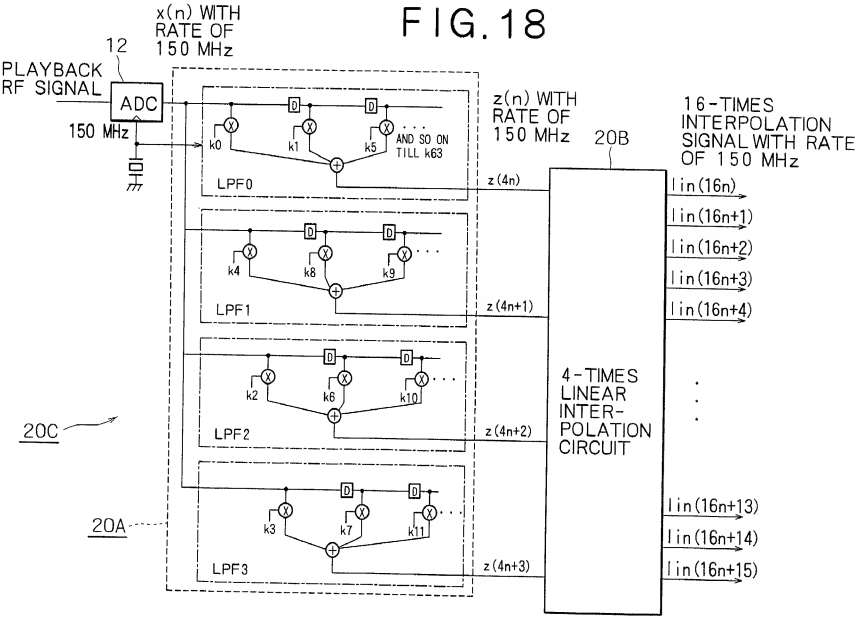

x(n) WITH RATE OF 150 MHz
12
PLAYBACK RF SIGNAL
ADC
150 MHz
k0
k1
k5
AND SO ON TILL k63
LPF0
k4
k8
k9
LPF1
k2
k6
k10
LPF2
k3
k7
k11
LPF3
z(n) WITH RATE OF 150 MHz
z(4n)
z(4n+1)
z(4n+2)
z(4n+3)
20B
4-TIMES LINEAR INTER-POLATION CIRCUIT
16-TIMES INTERPOLATION SIGNAL WITH RATE OF 150 MHz
lin(16n)
lin(16n+1)
lin(16n+2)
lin(16n+3)
lin(16n+4)
lin(16n+13)
lin(16n+14)
lin(16n+15)
20C
20A

FIG. 19

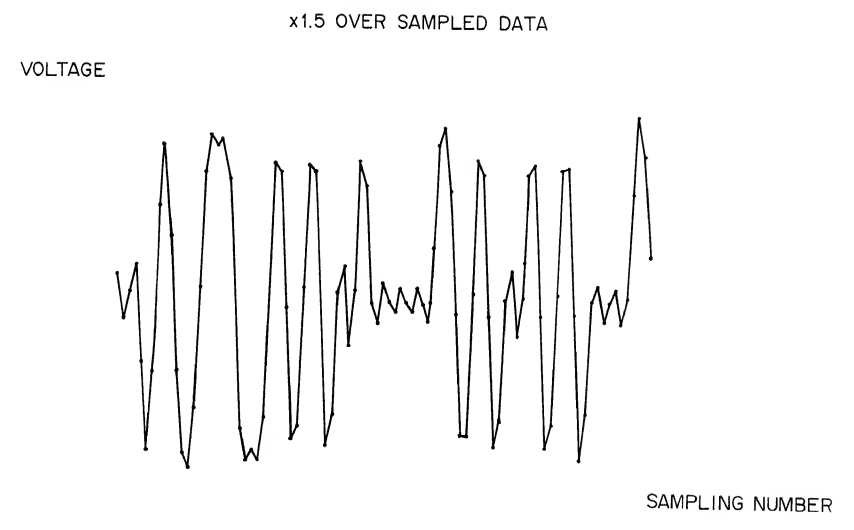
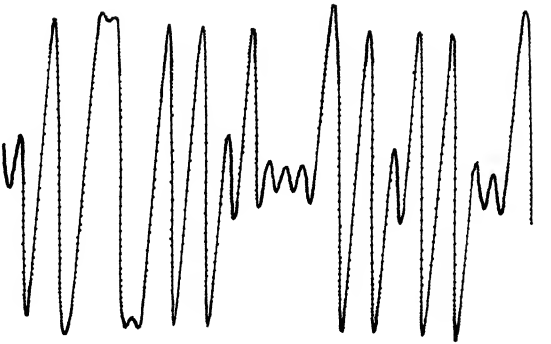


FIG. 20

x16 INTERPOLATED DATA

VOLTAGE



SAMPLING NUMBER

FIG. 21

EYE PATTERN OF THE x16 INTERPOLATED DATA

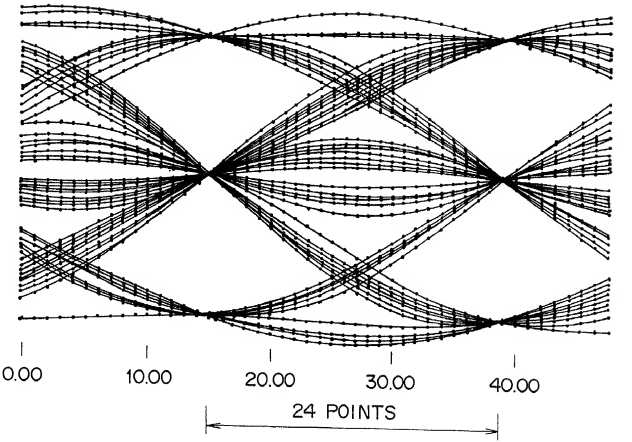


FIG. 22

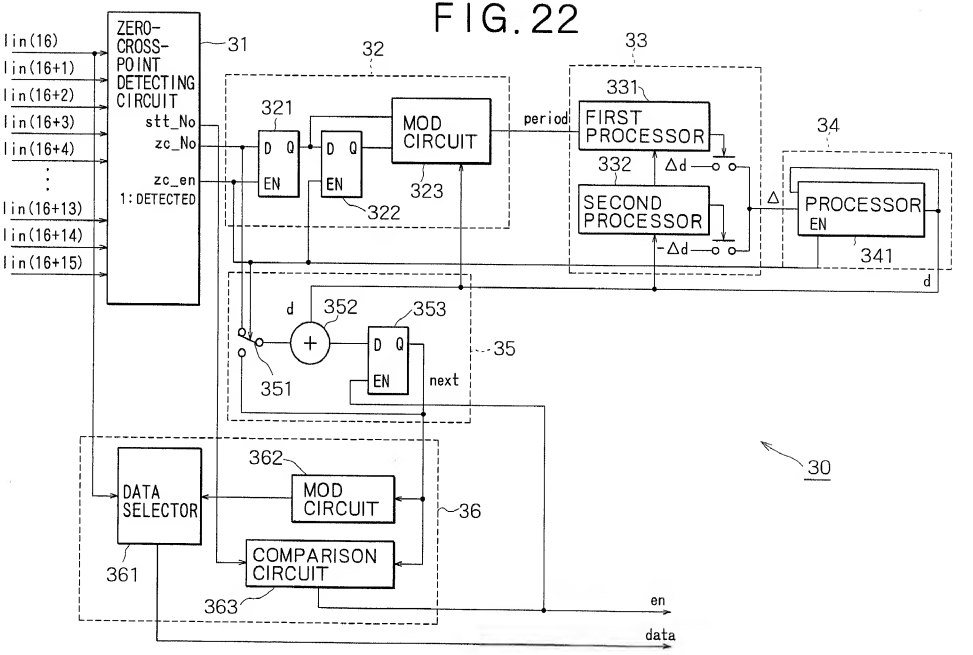

Iin(16)
Iin(16+1)
Iin(16+2)
Iin(16+3)
Iin(16+4)
Iin(16+13)
Iin(16+14)
Iin(16+15)
ZERO-CROSS-POINT DETECTING CIRCUIT
31
stt_No
zc_No
zc_en
1: DETECTED
32
321
D Q
EN
322
323
MOD CIRCUIT
period
33
331
FIRST PROCESSOR
332
SECOND PROCESSOR
Δd
-Δd
Δ
34
PROCESSOR
EN
341
d
352
353
351
35
next
30
362
DATA SELECTOR
MOD CIRCUIT
36
361
COMPARISON CIRCUIT
363
en
data

FIG. 23

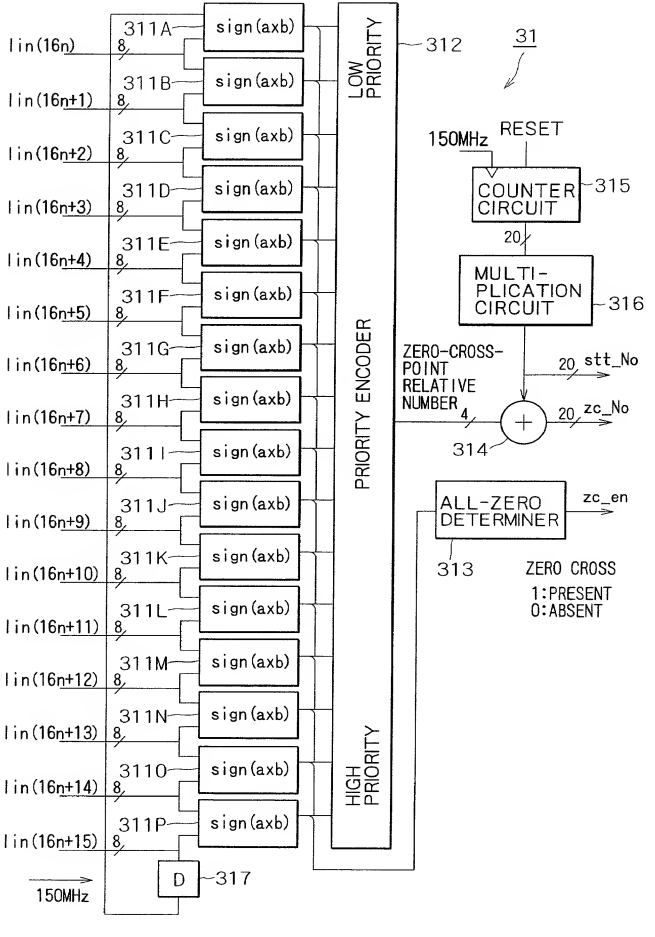

311A
311B
311C
311D
311E
311F
311G
311H
311I
311J
311K
311L
311M
311N
311O
311P
sign(axb)
Iin(16n)
Iin(16n+1)
Iin(16n+2)
Iin(16n+3)
Iin(16n+4)
Iin(16n+5)
Iin(16n+6)
Iin(16n+7)
Iin(16n+8)
Iin(16n+9)
Iin(16n+10)
Iin(16n+11)
Iin(16n+12)
Iin(16n+13)
Iin(16n+14)
Iin(16n+15)
8
LOW PRIORITY
PRIORITY ENCODER
HIGH PRIORITY
312
31
150MHz
RESET
COUNTER CIRCUIT
315
20
MULTI-PLICATION CIRCUIT
316
ZERO-CROSS-POINT RELATIVE NUMBER
4
20
stt_No
20
zc_No
314
ALL-ZERO DETERMINER
zc_en
313
ZERO CROSS
1:PRESENT
0:ABSENT
D
317
150MHz

FIG. 24

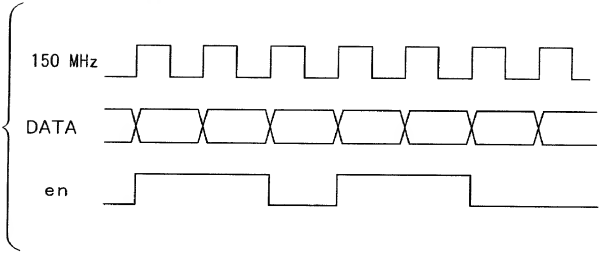

150 MHz
DATA
en

FIG. 25

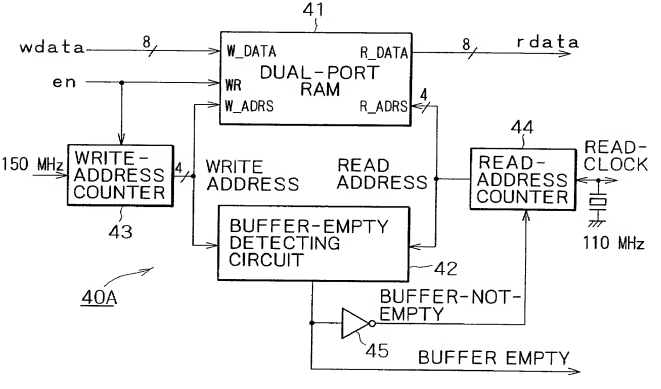

41
wdata
8
W_DATA
R_DATA
8
rdata
en
WR
DUAL-PORT RAM
W_ADRS
R_ADRS
4
44
150 MHz
WRITE-ADDRESS COUNTER
4
WRITE ADDRESS
READ ADDRESS
READ-ADDRESS COUNTER
READ-CLOCK
43
BUFFER-EMPTY DETECTING CIRCUIT
42
110 MHz
40A
BUFFER-NOT-EMPTY
45
BUFFER EMPTY

FIG. 26

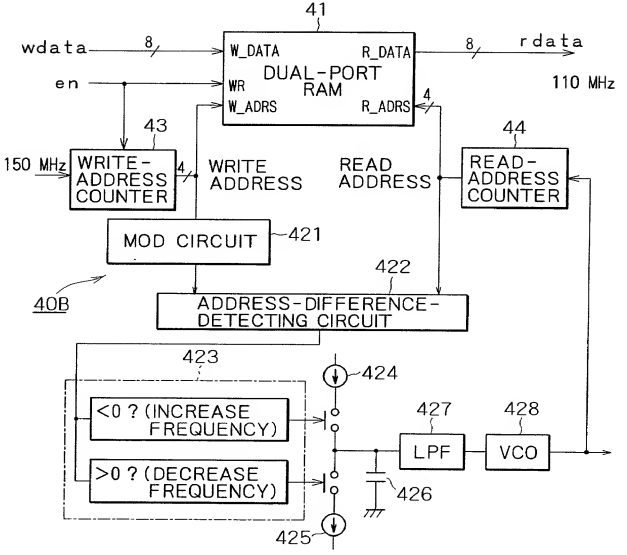


FIG. 27

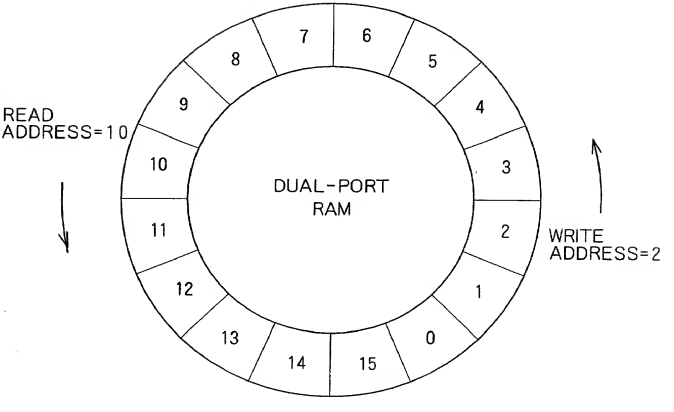


FIG. 28

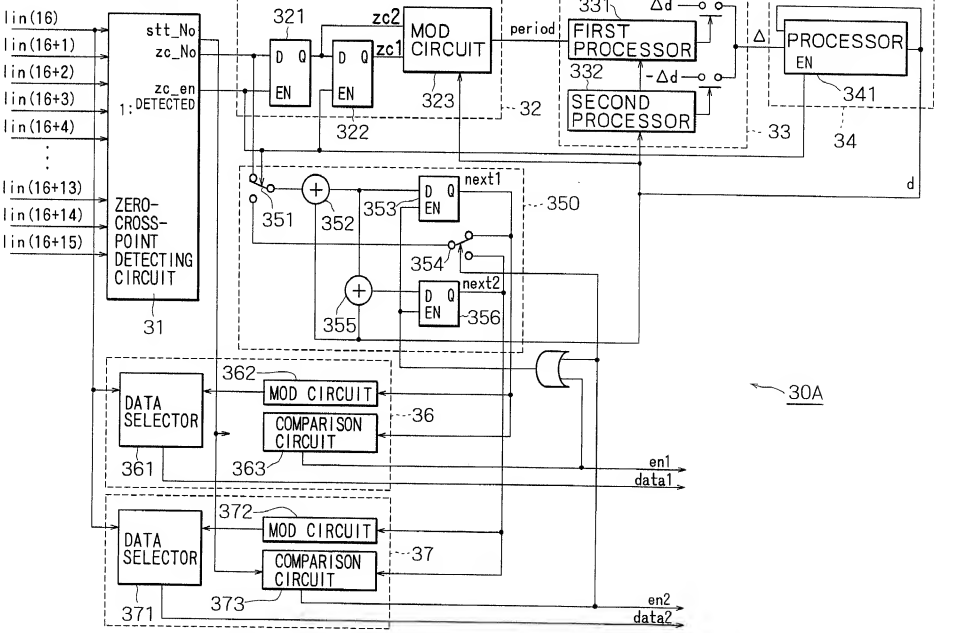

Iin(16)
Iin(16+1)
Iin(16+2)
Iin(16+3)
Iin(16+4)
Iin(16+13)
Iin(16+14)
Iin(16+15)
stt_No
zc_No
zc_en
1:DETECTED
ZERO-CROSS-POINT DETECTING CIRCUIT
31
321
zc2
zc1
D Q
EN
322
323
MOD CIRCUIT
period
32
331
FIRST PROCESSOR
332
SECOND PROCESSOR
Δd
-Δd
Δ
33
PROCESSOR
341
34
d
350
351
352
353
354
355
356
next1
next2
DATA SELECTOR
361
362
363
MOD CIRCUIT
COMPARISON CIRCUIT
36
en1
data1
371
372
373
37
en2
data2
30A

FIG. 29

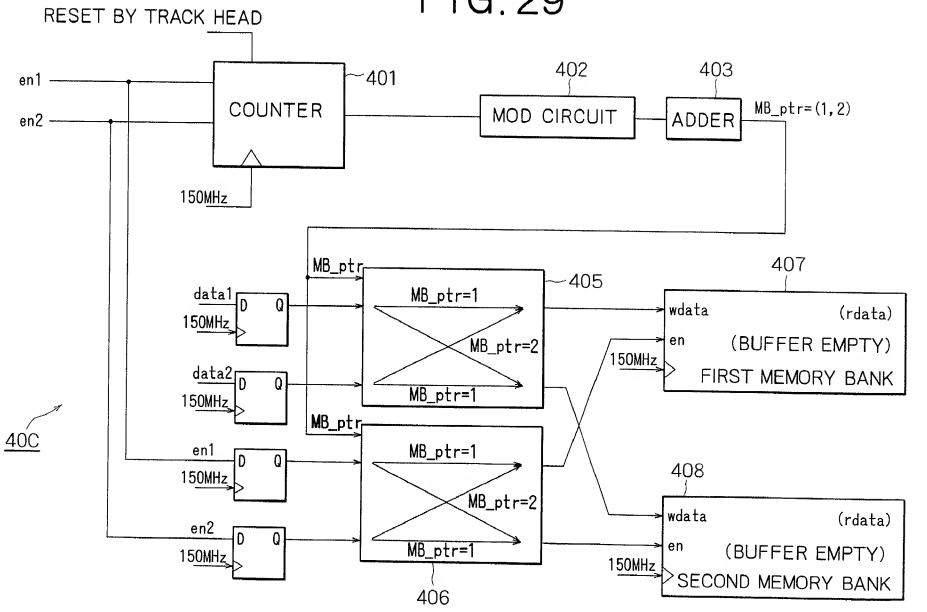

RESET BY TRACK HEAD
en1
en2
COUNTER
401
150MHz
402
MOD CIRCUIT
403
ADDER
MB_ptr=(1,2)
MB_ptr
405
data1
data2
D
Q
150MHz
MB_ptr=1
MB_ptr=2
MB_ptr=1
407
wdata
(rdata)
en
(BUFFER EMPTY)
FIRST MEMORY BANK
40C
en1
en2
MB_ptr
MB_ptr=1
MB_ptr=2
MB_ptr=1
406
408
wdata
(rdata)
en
(BUFFER EMPTY)
SECOND MEMORY BANK

FIG. 30A

⋮	⋮
⋮	⋮
⋮	⋮
ADDRESS 5	data(10)
ADDRESS 4	data(8)
ADDRESS 3	data(6)
ADDRESS 2	data(4)
ADDRESS 1	data(2)
ADDRESS 0	data(0)

FIRST MEMORY BANK

FIG. 30B

⋮	⋮
⋮	⋮
⋮	⋮
ADDRESS 5	data(11)
ADDRESS 4	data(9)
ADDRESS 3	data(7)
ADDRESS 2	data(5)
ADDRESS 1	data(3)
ADDRESS 0	data(1)

SECOND MEMORY BANK

FIG. 31

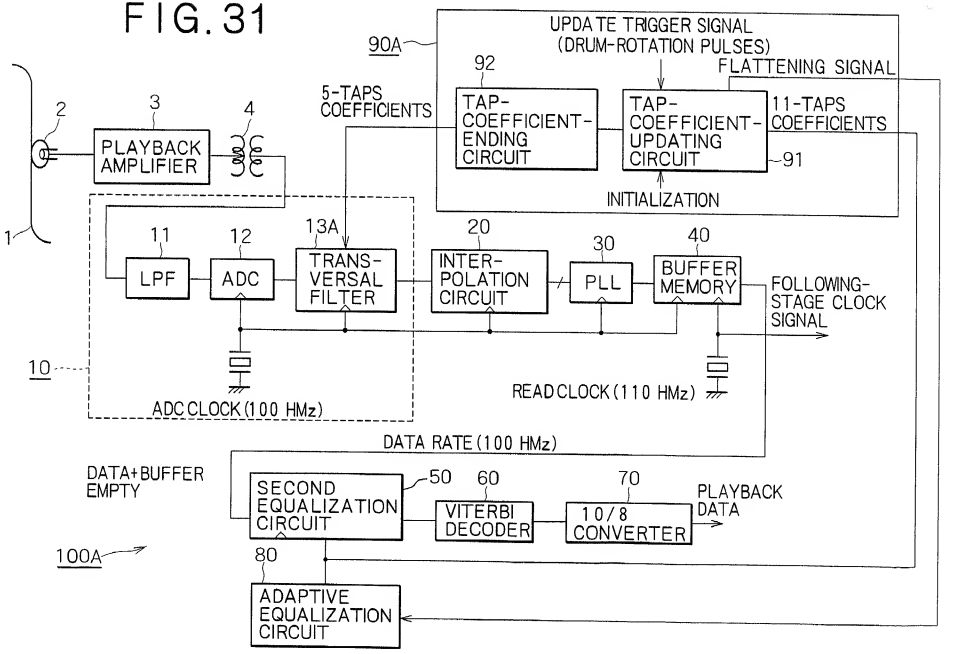

90A
UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
FLATTENING SIGNAL
92
5-TAPS
COEFFICIENTS
TAP-
COEFFICIENT-
ENDING
CIRCUIT
TAP-
COEFFICIENT-
UPDATING
CIRCUIT
11-TAPS
COEFFICIENTS
91
INITIALIZATION
2
3
4
PLAYBACK
AMPLIFIER
1
11
12
13A
20
30
40
LPF
ADC
TRANS-
VERSAL
FILTER
INTER-
POLATION
CIRCUIT
PLL
BUFFER
MEMORY
FOLLOWING-
STAGE CLOCK
SIGNAL
10
ADC CLOCK (100 HMz)
READ CLOCK (110 HMz)
DATA RATE (100 HMz)
DATA+BUFFER
EMPTY
SECOND
EQUALIZATION
CIRCUIT
50
60
70
VITERBI
DECODER
10/8
CONVERTER
PLAYBACK
DATA
100A
80
ADAPTIVE
EQUALIZATION
CIRCUIT

FIG. 32

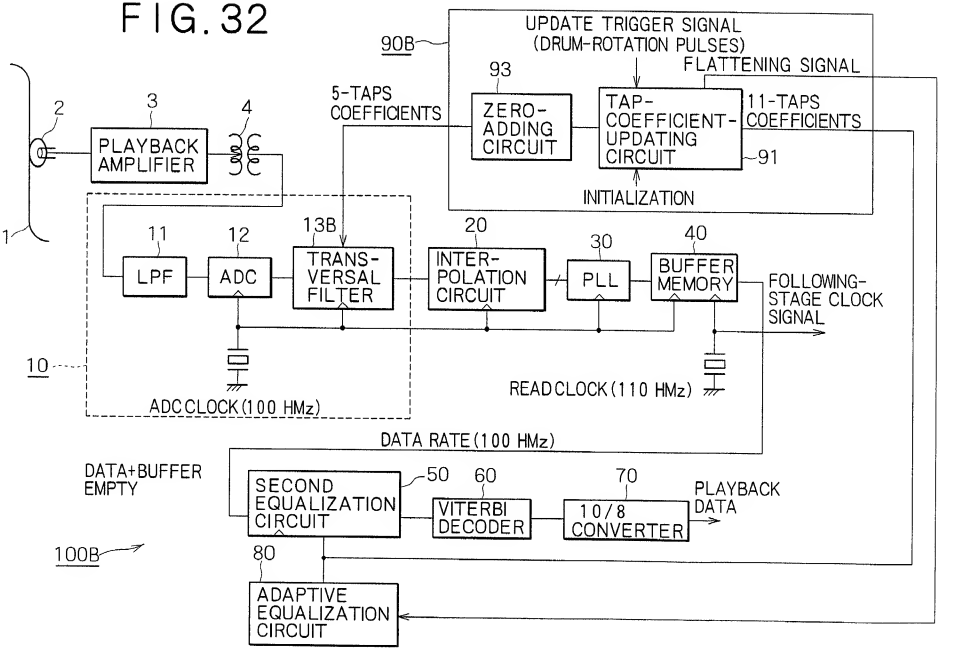

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
FLATTENING SIGNAL
90B
93
5-TAPS COEFFICIENTS
ZERO-ADDING CIRCUIT
TAP-COEFFICIENT-UPDATING CIRCUIT
11-TAPS COEFFICIENTS
91
INITIALIZATION
2
3
4
PLAYBACK AMPLIFIER
1
11
12
13B
20
30
40
LPF
ADC
TRANS-VERSAL FILTER
INTER-POLATION CIRCUIT
PLL
BUFFER MEMORY
FOLLOWING-STAGE CLOCK SIGNAL
10
ADC CLOCK (100 HMz)
READ CLOCK (110 HMz)
DATA RATE (100 HMz)
DATA+BUFFER EMPTY
50
60
70
SECOND EQUALIZATION CIRCUIT
VITERBI DECODER
10/8 CONVERTER
PLAYBACK DATA
100B
80
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 33

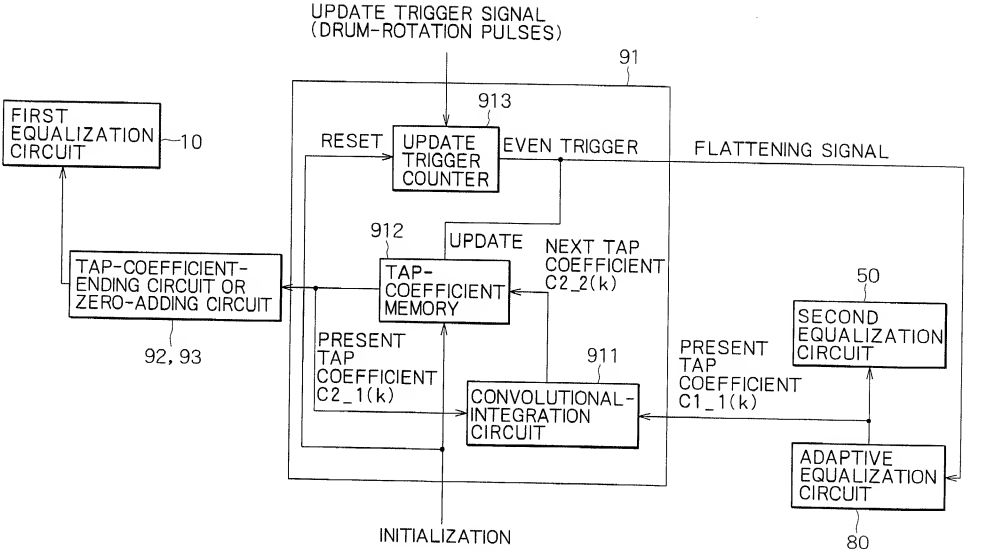
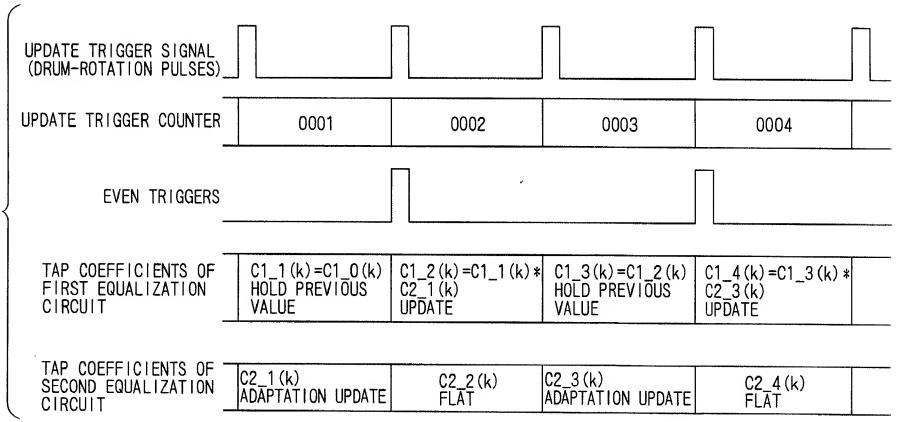
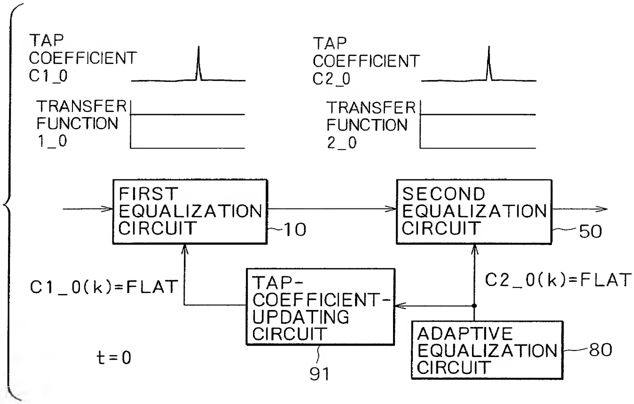

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
91
913
FIRST EQUALIZATION CIRCUIT
10
RESET
UPDATE TRIGGER COUNTER
EVEN TRIGGER
FLATTENING SIGNAL
912
UPDATE
NEXT TAP COEFFICIENT C2_2(k)
TAP-COEFFICIENT-ENDING CIRCUIT OR ZERO-ADDING CIRCUIT
92, 93
TAP-COEFFICIENT MEMORY
50
SECOND EQUALIZATION CIRCUIT
PRESENT TAP COEFFICIENT C2_1(k)
911
PRESENT TAP COEFFICIENT C1_1(k)
CONVOLUTIONAL-INTEGRATION CIRCUIT
ADAPTIVE EQUALIZATION CIRCUIT
80
INITIALIZATION

FIG. 34


UPDATE TRIGGER SIGNAL (DRUM-ROTATION PULSES)
UPDATE TRIGGER COUNTER
0001
0002
0003
0004
EVEN TRIGGERS
TAP COEFFICIENTS OF FIRST EQUALIZATION CIRCUIT
C1_1(k)=C1_0(k) HOLD PREVIOUS VALUE
C1_2(k)=C1_1(k)* C2_1(k) UPDATE
C1_3(k)=C1_2(k) HOLD PREVIOUS VALUE
C1_4(k)=C1_3(k)* C2_3(k) UPDATE
TAP COEFFICIENTS OF SECOND EQUALIZATION CIRCUIT
C2_1(k) ADAPTATION UPDATE
C2_2(k) FLAT
C2_3(k) ADAPTATION UPDATE
C2_4(k) FLAT

F I G. 35



F I G. 36

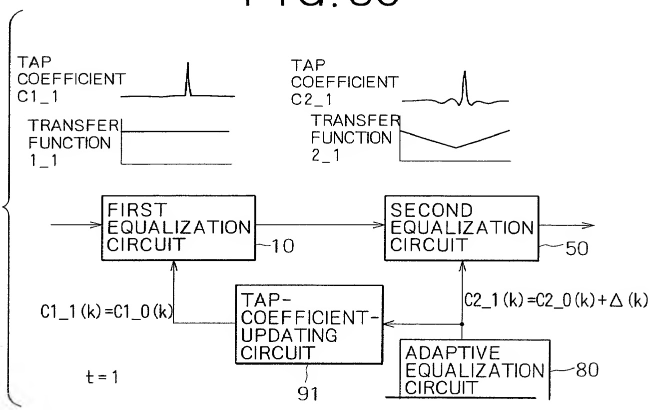


FIG. 37

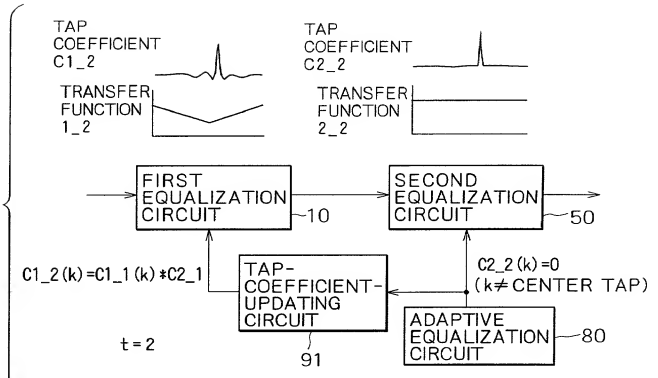


FIG. 38

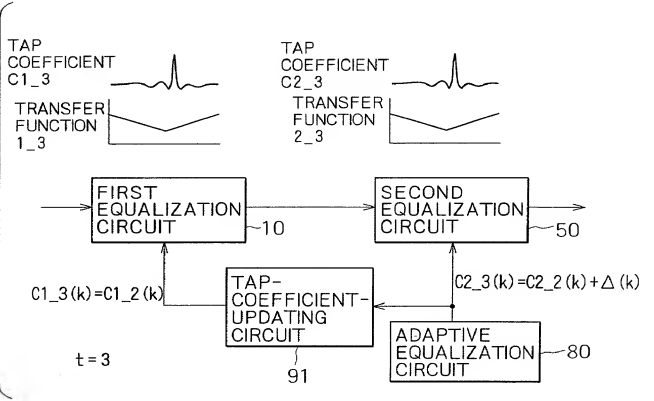


FIG. 39

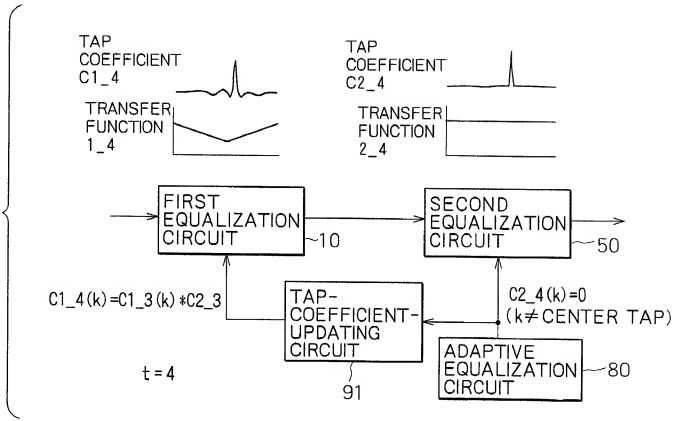


FIG. 40

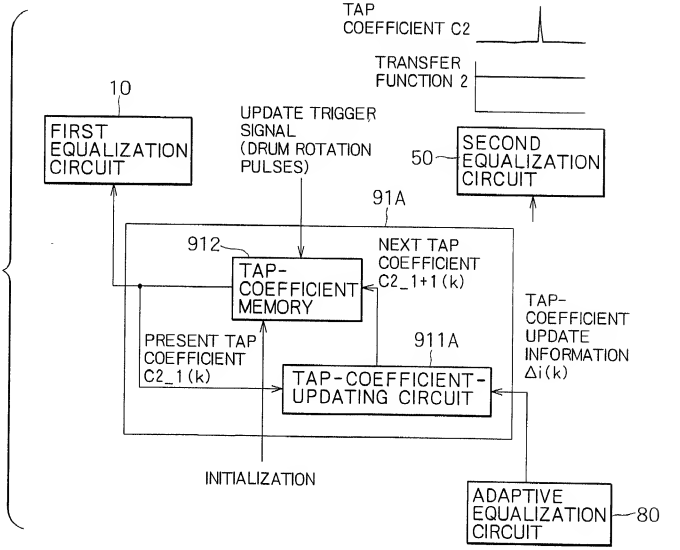

TAP
COEFFICIENT C2
TRANSFER
FUNCTION 2
10
FIRST
EQUALIZATION
CIRCUIT
UPDATE TRIGGER
SIGNAL
(DRUM ROTATION
PULSES)
50
SECOND
EQUALIZATION
CIRCUIT
91A
912
TAP-
COEFFICIENT
MEMORY
NEXT TAP
COEFFICIENT
C2_1+1(k)
TAP-
COEFFICIENT
UPDATE
INFORMATION
Δi(k)
PRESENT TAP
COEFFICIENT
C2_1(k)
911A
TAP-COEFFICIENT-
UPDATING CIRCUIT
INITIALIZATION
ADAPTIVE
EQUALIZATION
CIRCUIT
80

FIG. 41

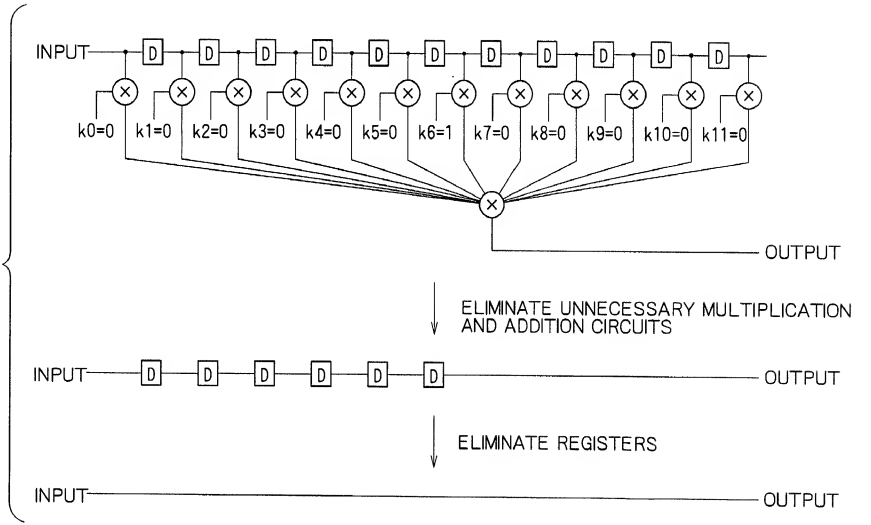

INPUT
D
k0=0
k1=0
k2=0
k3=0
k4=0
k5=0
k6=1
k7=0
k8=0
k9=0
k10=0
k11=0
OUTPUT
ELIMINATE UNNECESSARY MULTIPLICATION AND ADDITION CIRCUITS
INPUT
OUTPUT
ELIMINATE REGISTERS
INPUT
OUTPUT

FIG. 42

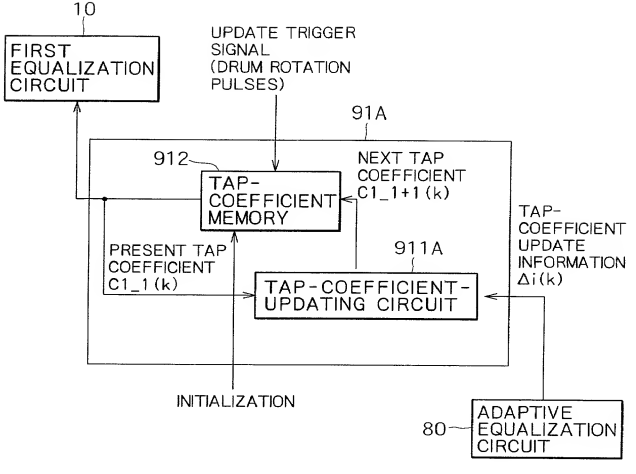

10
FIRST EQUALIZATION CIRCUIT
UPDATE TRIGGER SIGNAL (DRUM ROTATION PULSES)
91A
912
TAP-COEFFICIENT MEMORY
NEXT TAP COEFFICIENT C1_1+1(k)
TAP-COEFFICIENT UPDATE INFORMATION Δi(k)
PRESENT TAP COEFFICIENT C1_1(k)
911A
TAP-COEFFICIENT-UPDATING CIRCUIT
INITIALIZATION
80
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 43

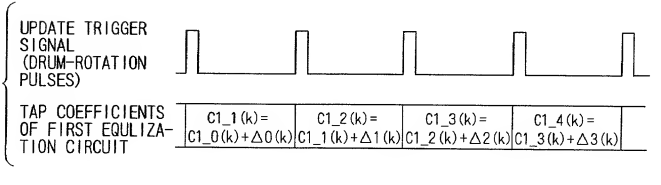

UPDATE TRIGGER SIGNAL (DRUM-ROTATION PULSES)
TAP COEFFICIENTS OF FIRST EQULIZATION CIRCUIT
C1_1(k)= C1_0(k)+Δ0(k)
C1_2(k)= C1_1(k)+Δ1(k)
C1_3(k)= C1_2(k)+Δ2(k)
C1_4(k)= C1_3(k)+Δ3(k)

FIG. 44

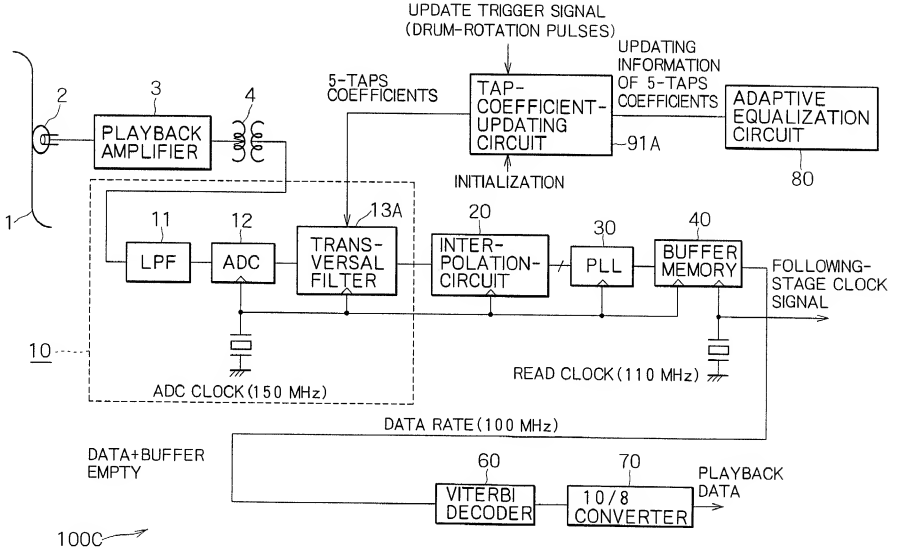

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
UPDATING INFORMATION OF 5-TAPS COEFFICIENTS
5-TAPS COEFFICIENTS
TAP-COEFFICIENT-UPDATING CIRCUIT
91A
ADAPTIVE EQUALIZATION CIRCUIT
80
INITIALIZATION
2
3
4
PLAYBACK AMPLIFIER
1
11
12
13A
LPF
ADC
TRANS-VERSAL FILTER
20
INTER-POLATION-CIRCUIT
30
PLL
40
BUFFER MEMORY
FOLLOWING-STAGE CLOCK SIGNAL
10
ADC CLOCK (150 MHz)
READ CLOCK (110 MHz)
DATA RATE (100 MHz)
DATA+BUFFER EMPTY
60
70
PLAYBACK DATA
VITERBI DECODER
10/8 CONVERTER
100C

FIG. 45

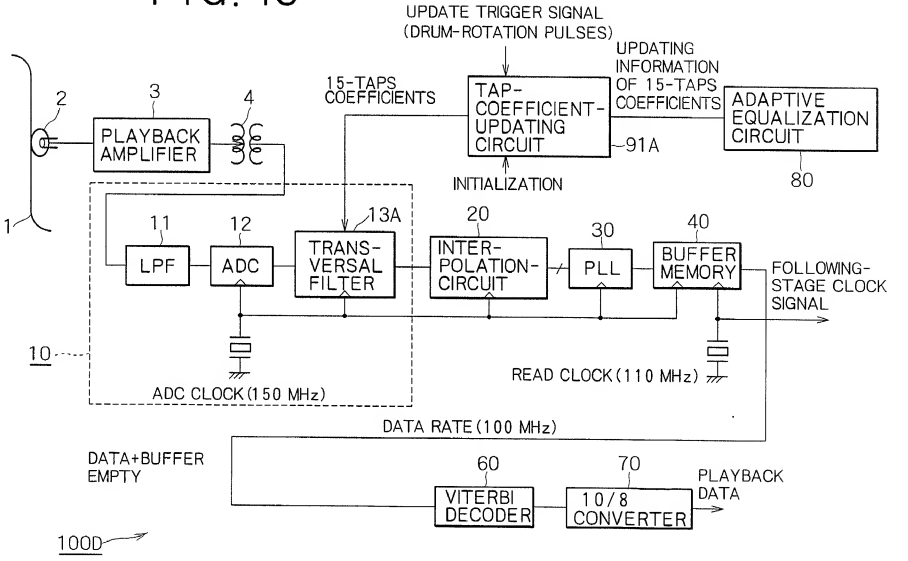

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
UPDATING
INFORMATION
OF 15-TAPS
COEFFICIENTS
15-TAPS
COEFFICIENTS
TAP-
COEFFICIENT-
UPDATING
CIRCUIT
91A
ADAPTIVE
EQUALIZATION
CIRCUIT
80
INITIALIZATION
2
3
4
PLAYBACK
AMPLIFIER
1
11
12
13A
20
30
40
LPF
ADC
TRANS-
VERSAL
FILTER
INTER-
POLATION-
CIRCUIT
PLL
BUFFER
MEMORY
FOLLOWING-
STAGE CLOCK
SIGNAL
10
ADC CLOCK(150 MHz)
READ CLOCK(110 MHz)
DATA RATE(100 MHz)
DATA+BUFFER
EMPTY
60
70
PLAYBACK
DATA
VITERBI
DECODER
10/8
CONVERTER
100D

FIG. 46A

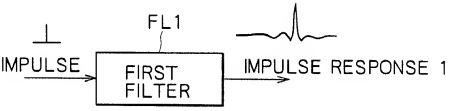


FIG. 46B

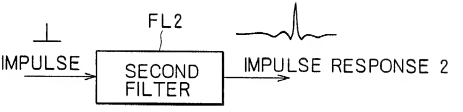


FIG. 46C

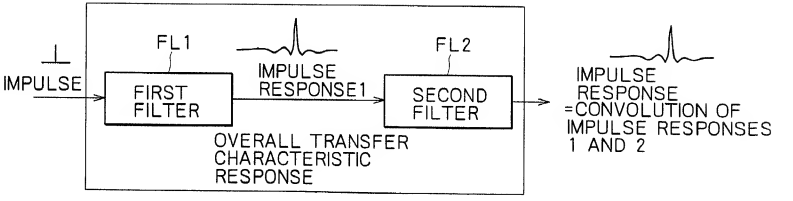


FIG. 47

TRANSFER CHARACTERISTICS OF THE 24-TAPS EQUALIZER 1 (t = i)

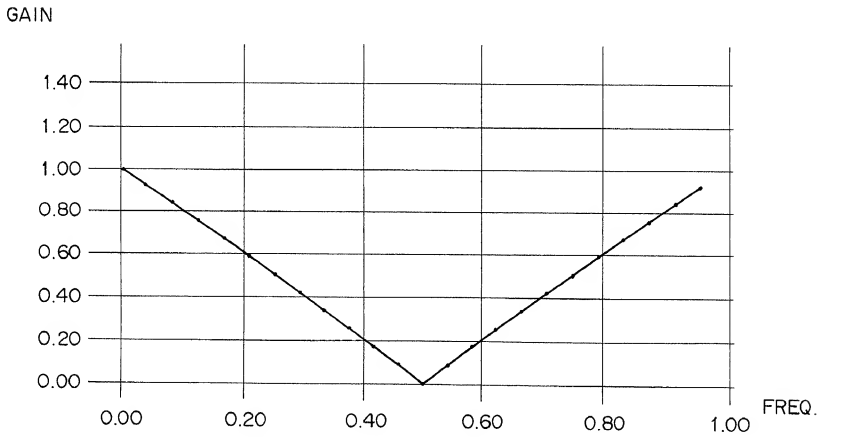


FIG. 48

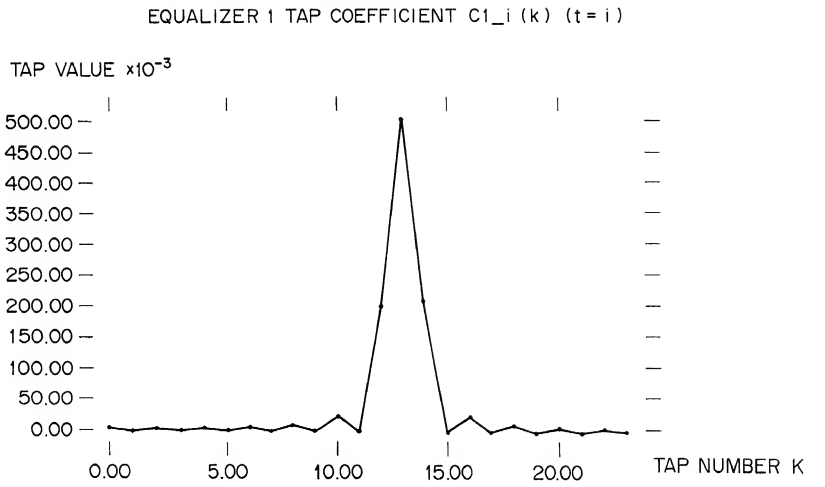

EQUALIZER 1 TAP COEFFICIENT C1_i (k) (t = i)
TAP VALUE x10^-3
500.00
450.00
400.00
350.00
300.00
250.00
200.00
150.00
100.00
50.00
0.00
0.00
5.00
10.00
15.00
20.00
TAP NUMBER K

FIG. 49

TRANSFER CHARACTERISTICS OF THE 24-TAPS EQUALIZER 2 (t = i)

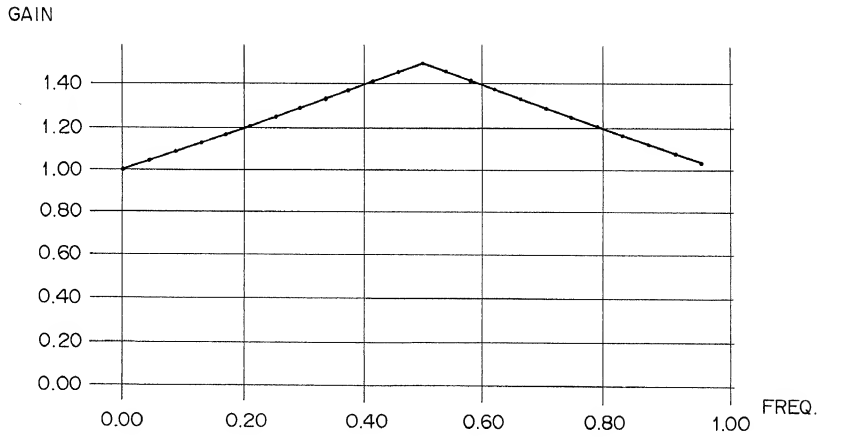


FIG. 50

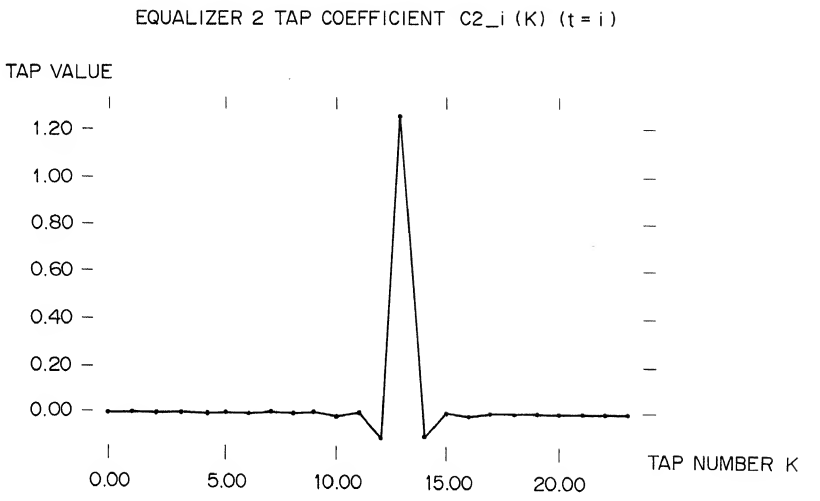

EQUALIZER 2 TAP COEFFICIENT C2_i (K) (t = i)
TAP VALUE
1.20
1.00
0.80
0.60
0.40
0.20
0.00
0.00
5.00
10.00
15.00
20.00
TAP NUMBER K

FIG. 51

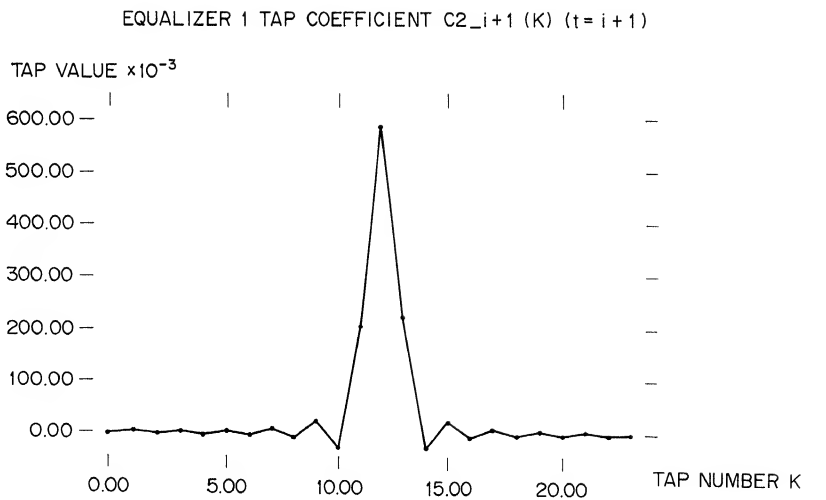

EQUALIZER 1 TAP COEFFICIENT C2_i+1 (K) (t = i + 1)
TAP VALUE x10^-3
600.00
500.00
400.00
300.00
200.00
100.00
0.00
0.00
5.00
10.00
15.00
20.00
TAP NUMBER K

FIG. 52

TRANSFER CHARACTERISTICS OF THE 24-TAPS EQUALIZER 1 (t = i+1)

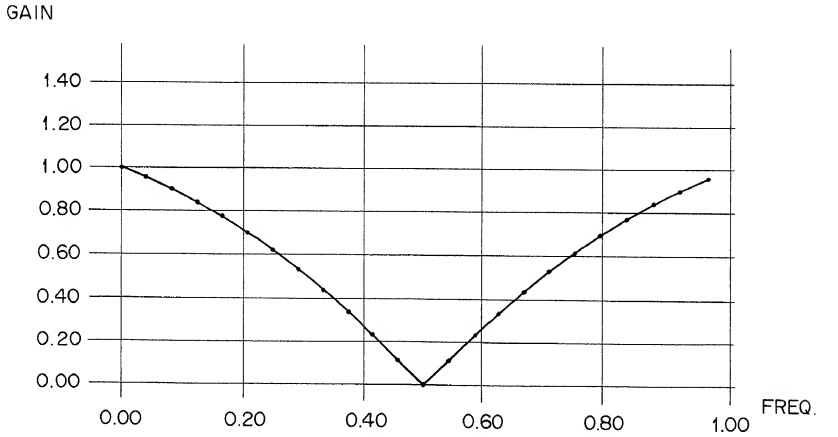


FIG. 53

TRANSFER CHARACTERISTICS OF THE 24-TAPS EQUALIZER 1 (t = i+1)

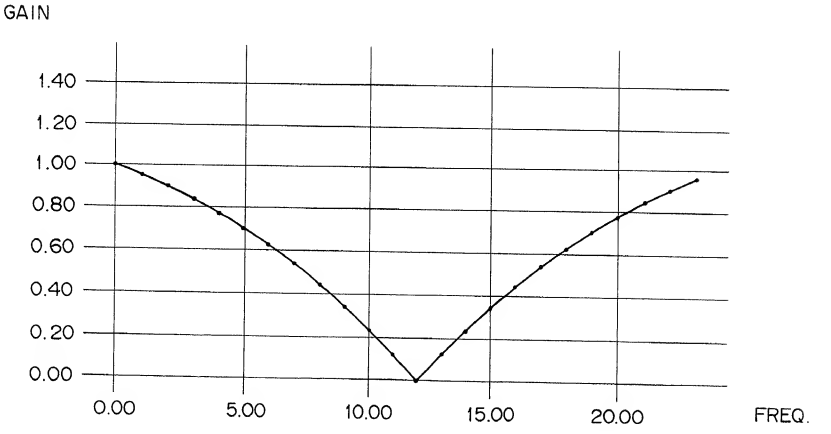


FIG. 54

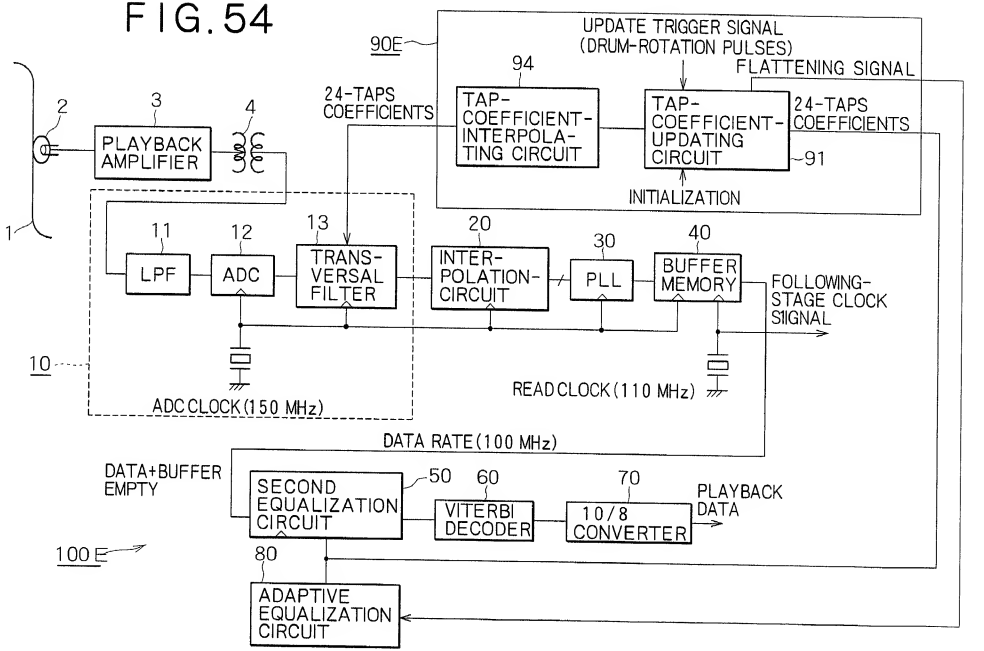

90E
UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
FLATTENING SIGNAL
94
24-TAPS COEFFICIENTS
TAP-COEFFICIENT-INTERPOLATING CIRCUIT
TAP-COEFFICIENT-UPDATING CIRCUIT
24-TAPS COEFFICIENTS
91
INITIALIZATION
2
3
4
PLAYBACK AMPLIFIER
1
11
12
13
LPF
ADC
TRANSVERSAL FILTER
20
INTERPOLATION-CIRCUIT
30
PLL
40
BUFFER MEMORY
FOLLOWING-STAGE CLOCK SIGNAL
10
ADC CLOCK (150 MHz)
READ CLOCK (110 MHz)
DATA RATE (100 MHz)
DATA+BUFFER EMPTY
SECOND EQUALIZATION CIRCUIT
50
60
VITERBI DECODER
70
10/8 CONVERTER
PLAYBACK DATA
100E
80
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 55

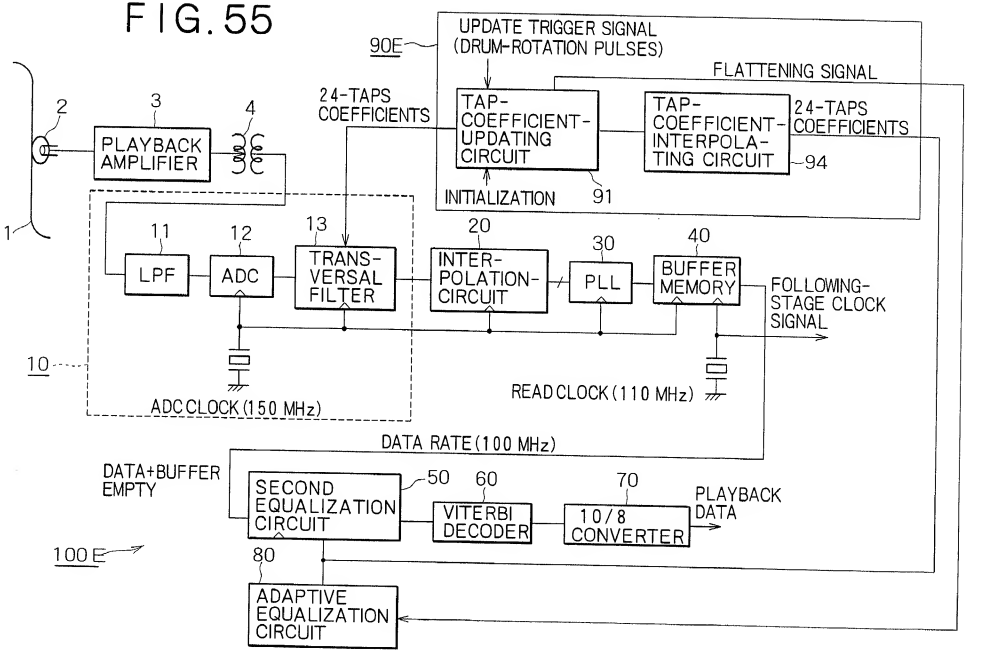

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
90E
FLATTENING SIGNAL
24-TAPS COEFFICIENTS
TAP-COEFFICIENT-UPDATING CIRCUIT
TAP-COEFFICIENT-INTERPOLATING CIRCUIT
24-TAPS COEFFICIENTS
94
INITIALIZATION
91
2
3
4
PLAYBACK AMPLIFIER
1
11
12
13
LPF
ADC
TRANSVERSAL FILTER
20
INTERPOLATION-CIRCUIT
30
PLL
40
BUFFER MEMORY
FOLLOWING-STAGE CLOCK SIGNAL
10
ADC CLOCK (150 MHz)
READ CLOCK (110 MHz)
DATA RATE (100 MHz)
DATA+BUFFER EMPTY
50
60
70
SECOND EQUALIZATION CIRCUIT
VITERBI DECODER
10/8 CONVERTER
PLAYBACK DATA
100E
80
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 56

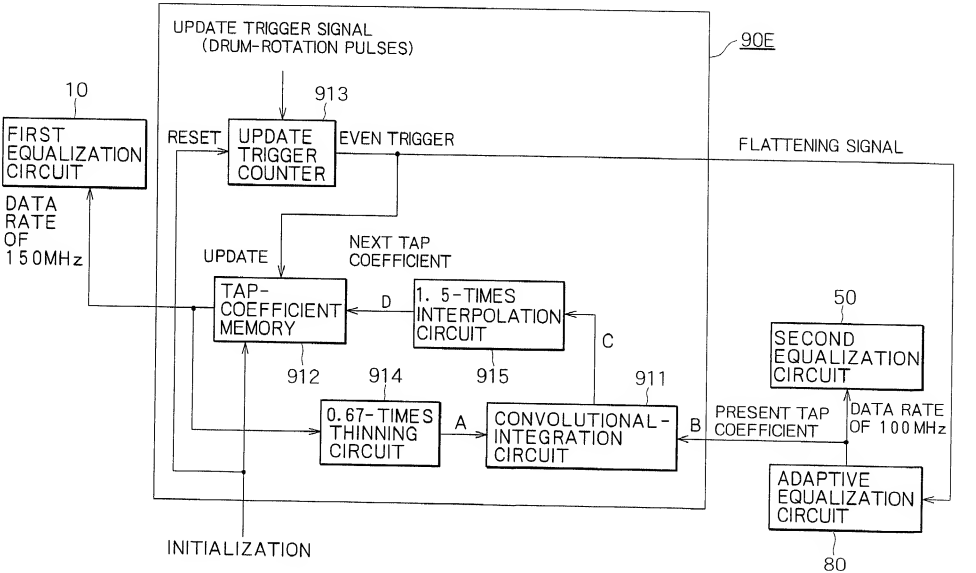

UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
90E
10
913
FIRST EQUALIZATION CIRCUIT
RESET
UPDATE TRIGGER COUNTER
EVEN TRIGGER
FLATTENING SIGNAL
DATA RATE OF 150MHz
UPDATE
NEXT TAP COEFFICIENT
TAP-COEFFICIENT MEMORY
D
1. 5-TIMES INTERPOLATION CIRCUIT
C
50
SECOND EQUALIZATION CIRCUIT
912
914
915
911
0.67-TIMES THINNING CIRCUIT
A
CONVOLUTIONAL-INTEGRATION CIRCUIT
B
PRESENT TAP COEFFICIENT
DATA RATE OF 100MHz
ADAPTIVE EQUALIZATION CIRCUIT
INITIALIZATION
80

FIG. 57

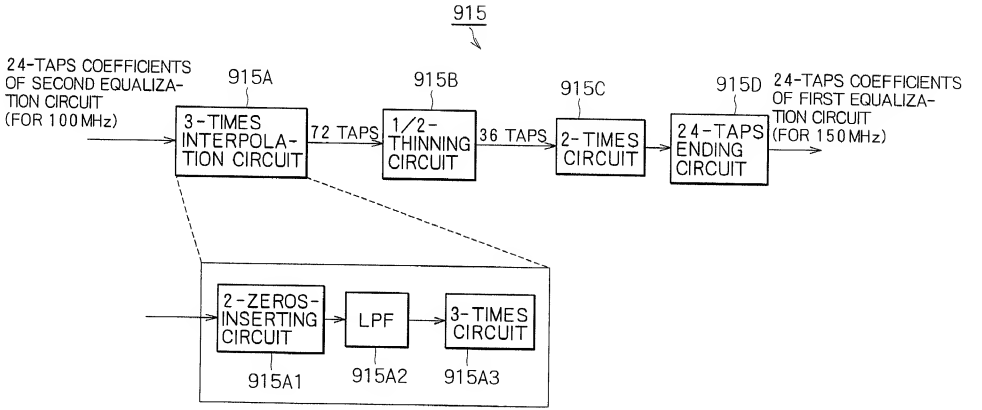

915
24-TAPS COEFFICIENTS OF SECOND EQUALIZATION CIRCUIT (FOR 100MHz)
915A
3-TIMES INTERPOLATION CIRCUIT
72 TAPS
915B
1/2-THINNING CIRCUIT
36 TAPS
915C
2-TIMES CIRCUIT
915D
24-TAPS ENDING CIRCUIT
24-TAPS COEFFICIENTS OF FIRST EQUALIZATION CIRCUIT (FOR 150MHz)
2-ZEROS-INSERTING CIRCUIT
915A1
LPF
915A2
3-TIMES CIRCUIT
915A3

FIG. 58

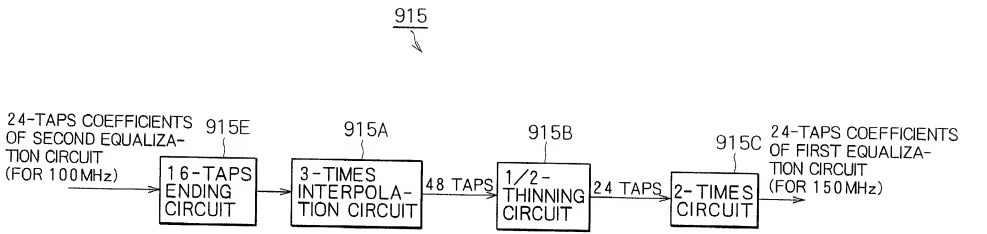

915
24-TAPS COEFFICIENTS OF SECOND EQUALIZATION CIRCUIT (FOR 100MHz)
915E
16-TAPS ENDING CIRCUIT
915A
3-TIMES INTERPOLATION CIRCUIT
48 TAPS
915B
1/2-THINNING CIRCUIT
24 TAPS
915C
2-TIMES CIRCUIT
24-TAPS COEFFICIENTS OF FIRST EQUALIZATION CIRCUIT (FOR 150MHz)

FIG. 59

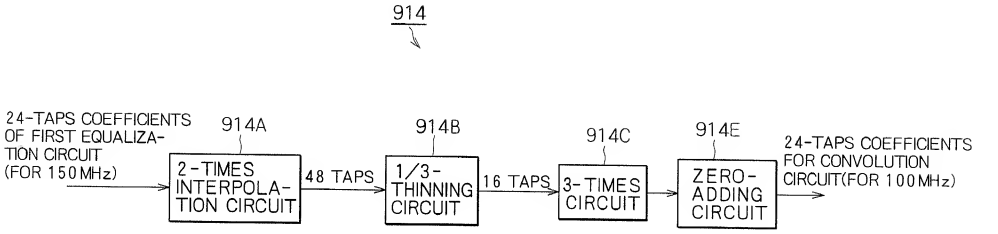

914
24-TAPS COEFFICIENTS OF FIRST EQUALIZATION CIRCUIT (FOR 150 MHz)
914A
2-TIMES INTERPOLATION CIRCUIT
48 TAPS
914B
1/3-THINNING CIRCUIT
16 TAPS
914C
3-TIMES CIRCUIT
914E
ZERO-ADDING CIRCUIT
24-TAPS COEFFICIENTS FOR CONVOLUTION CIRCUIT(FOR 100 MHz)

FIG. 60

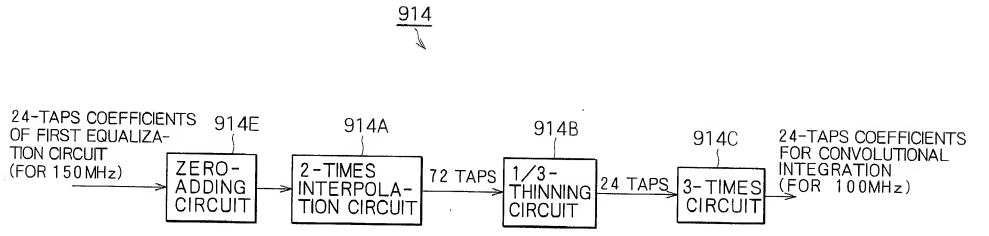

914
24-TAPS COEFFICIENTS OF FIRST EQUALIZATION CIRCUIT (FOR 150MHz)
914E
ZERO-ADDING CIRCUIT
914A
2-TIMES INTERPOLATION CIRCUIT
72 TAPS
914B
1/3-THINNING CIRCUIT
24 TAPS
914C
3-TIMES CIRCUIT
24-TAPS COEFFICIENTS FOR CONVOLUTIONAL INTEGRATION (FOR 100MHz)

FIG. 61

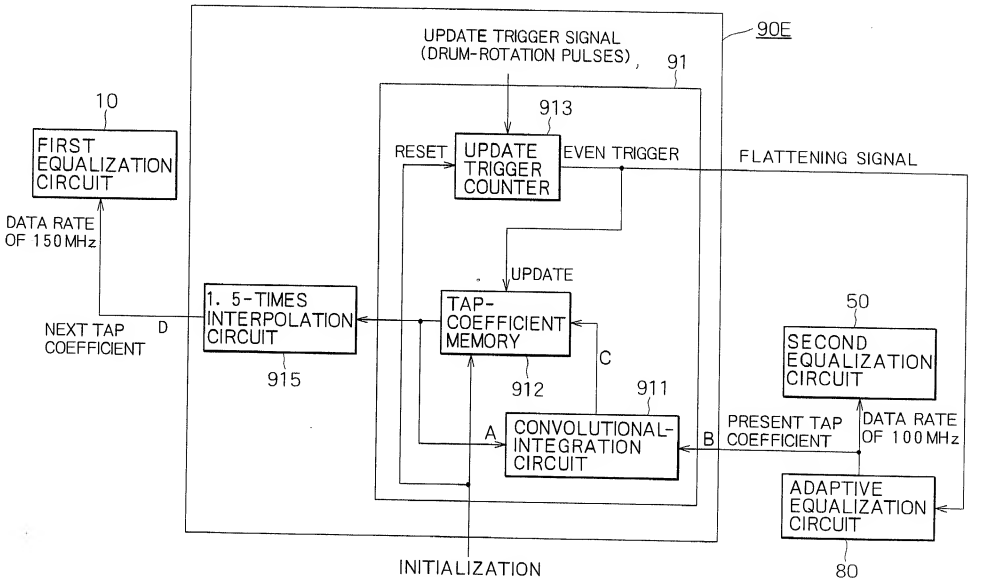


FIG. 62

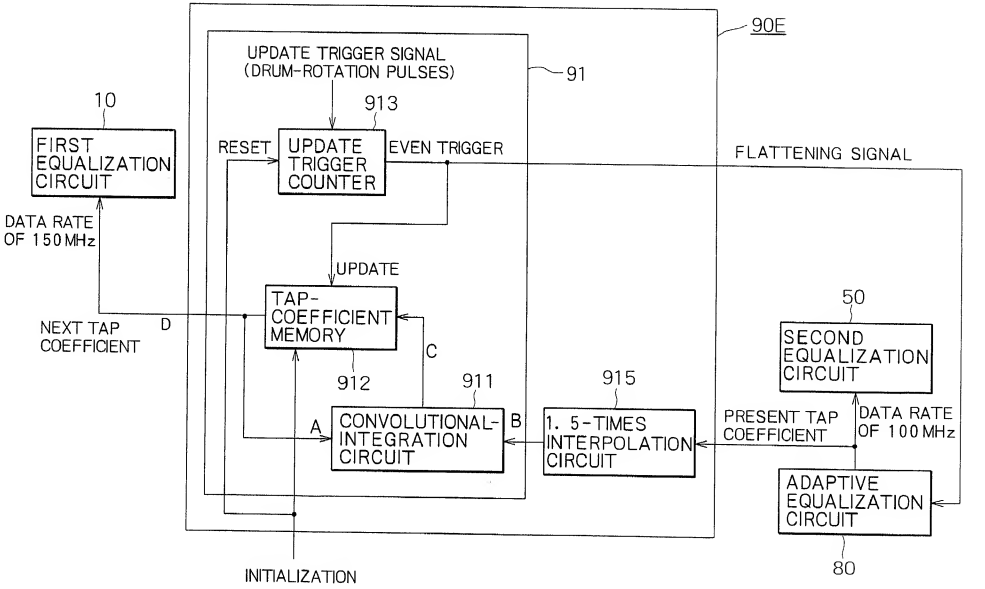


FIG. 63

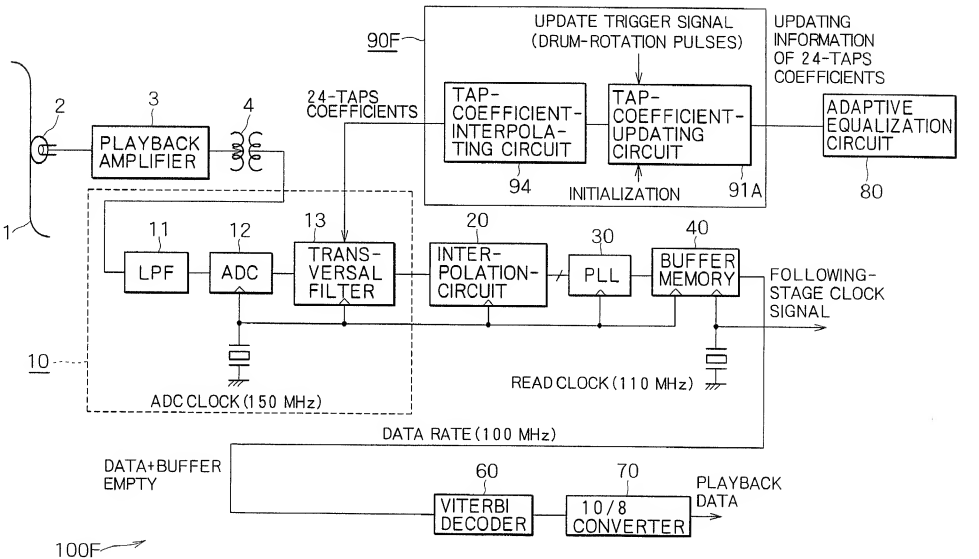

90F
UPDATE TRIGGER SIGNAL
(DRUM-ROTATION PULSES)
UPDATING
INFORMATION
OF 24-TAPS
COEFFICIENTS
2
3
4
PLAYBACK
AMPLIFIER
24-TAPS
COEFFICIENTS
TAP-
COEFFICIENT-
INTERPOLA-
TING CIRCUIT
94
TAP-
COEFFICIENT-
UPDATING
CIRCUIT
INITIALIZATION
91A
ADAPTIVE
EQUALIZATION
CIRCUIT
80
1
11
12
13
20
30
40
LPF
ADC
TRANS-
VERSAL
FILTER
INTER-
POLATION-
CIRCUIT
PLL
BUFFER
MEMORY
FOLLOWING-
STAGE CLOCK
SIGNAL
10
ADC CLOCK (150 MHz)
READ CLOCK (110 MHz)
DATA RATE (100 MHz)
DATA+BUFFER
EMPTY
60
70
VITERBI
DECODER
10/8
CONVERTER
PLAYBACK
DATA
100F

FIG. 64

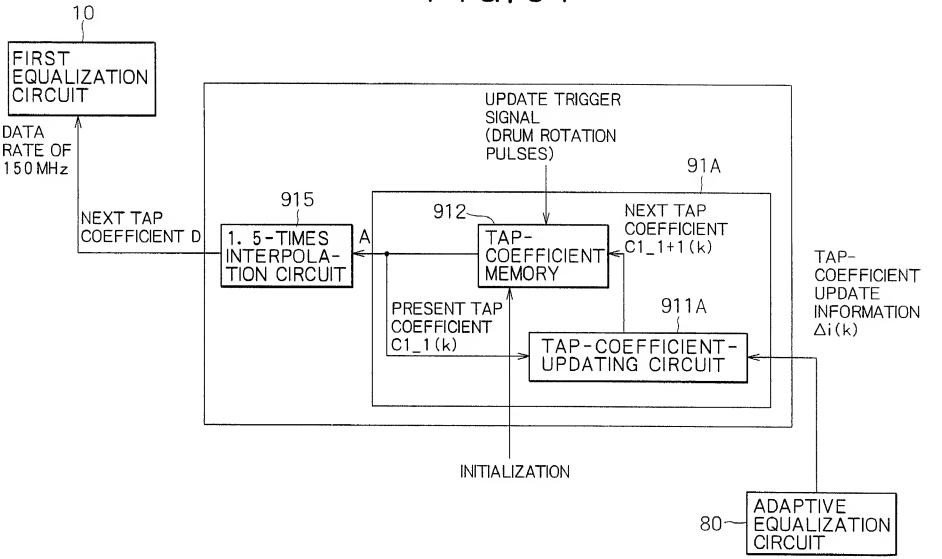


FIG. 65

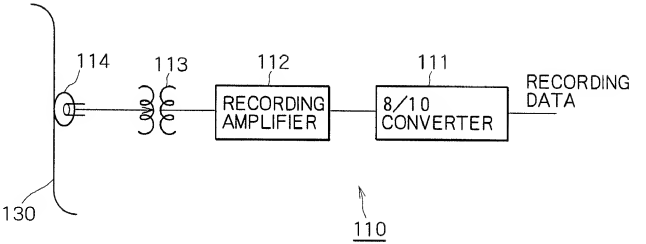

114
113
112
111
RECORDING AMPLIFIER
8/10 CONVERTER
RECORDING DATA
130
110

FIG. 66

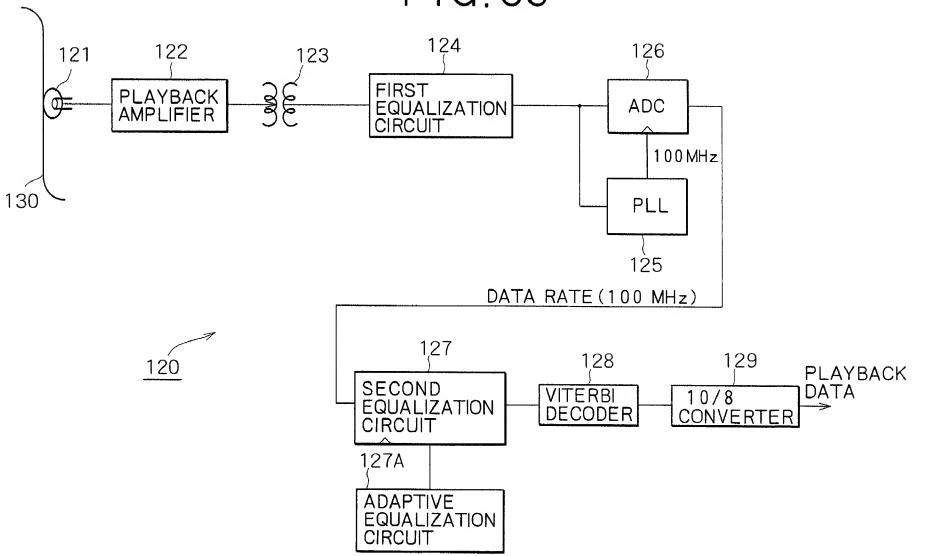

121
122
123
124
126
PLAYBACK AMPLIFIER
FIRST EQUALIZATION CIRCUIT
ADC
100MHz
PLL
125
130
DATA RATE (100 MHz)
120
127
128
129
SECOND EQUALIZATION CIRCUIT
VITERBI DECODER
10/8 CONVERTER
PLAYBACK DATA
127A
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 67

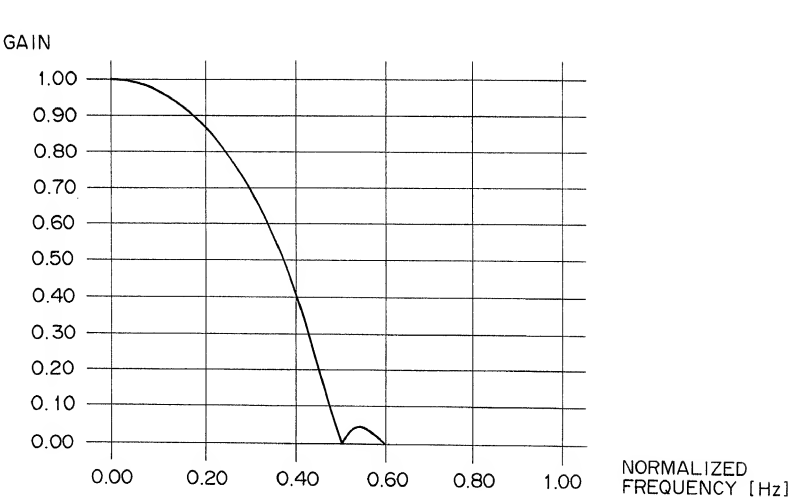

PR1 CHANNEL CHARACTERISTICS
GAIN
1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
0.00
0.20
0.40
0.60
0.80
1.00
NORMALIZED FREQUENCY [Hz]

FIG. 68

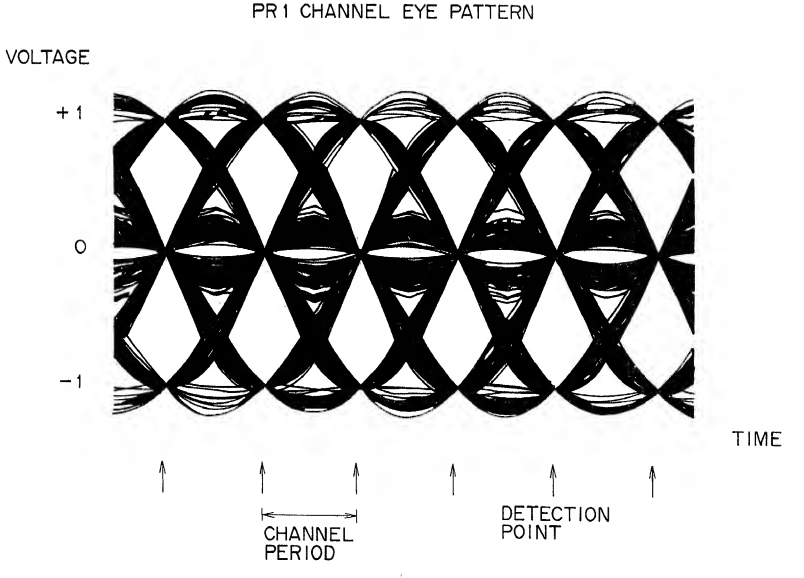
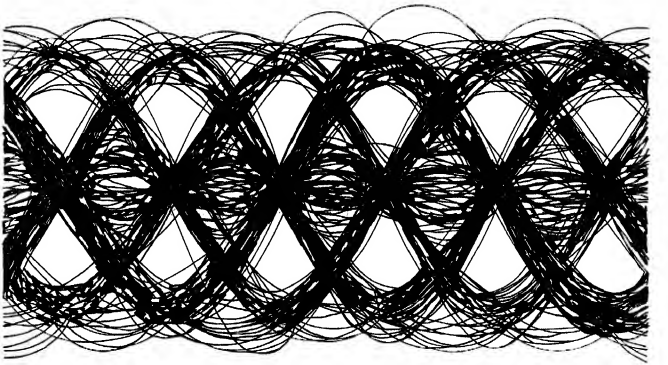

PR1 CHANNEL EYE PATTERN
VOLTAGE
+1
0
-1
TIME
CHANNEL PERIOD
DETECTION POINT

FIG. 69

PR1 CHANNEL EYE PATTERN

VOLTAGE

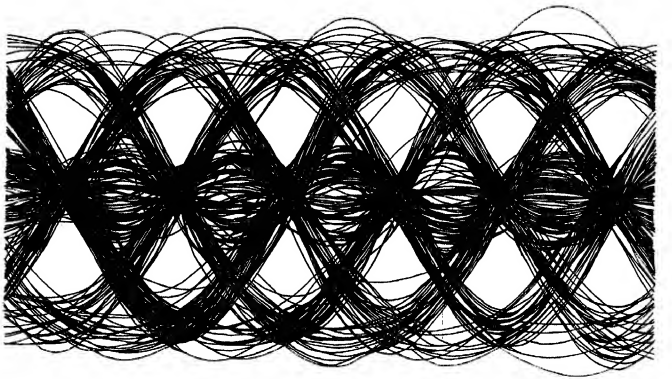


TIME

FIG. 70

PR1 CHANNEL EYE PATTERN

VOLTAGE



TIME

FIG. 71

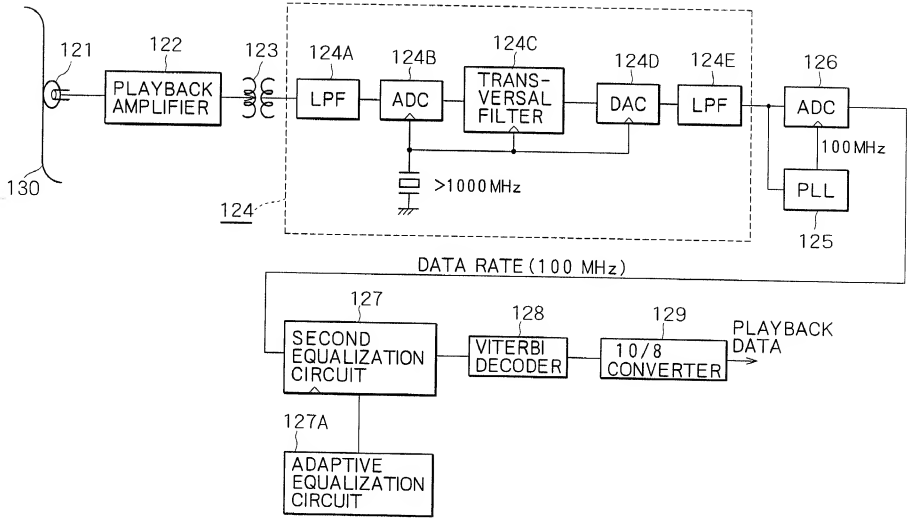

121
122
123
124A
124B
124C
124D
124E
126
PLAYBACK AMPLIFIER
LPF
ADC
TRANS-VERSAL FILTER
DAC
LPF
ADC
100MHz
PLL
125
130
124
>1000MHz
DATA RATE (100 MHz)
127
SECOND EQUALIZATION CIRCUIT
128
VITERBI DECODER
129
10/8 CONVERTER
PLAYBACK DATA
127A
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 72

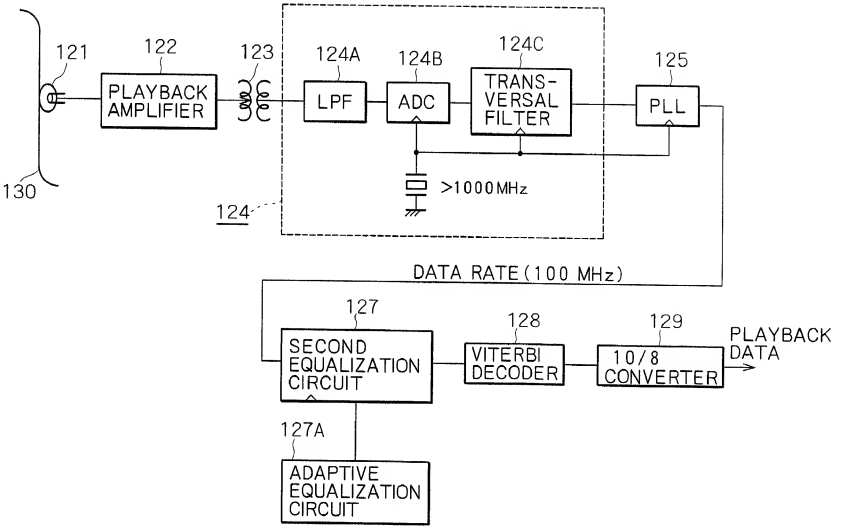
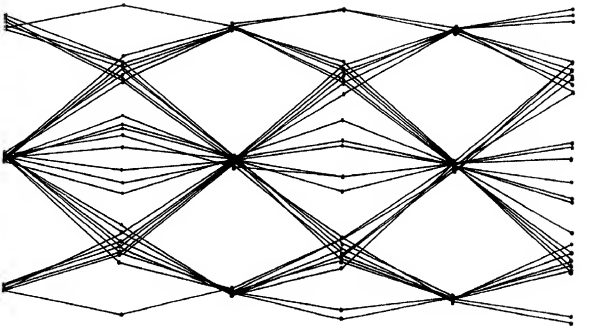

121
122
123
124A
124B
124C
125
PLAYBACK AMPLIFIER
LPF
ADC
TRANS-VERSAL FILTER
PLL
130
124
>1000MHz
DATA RATE(100 MHz)
127
128
129
PLAYBACK DATA
SECOND EQUALIZATION CIRCUIT
VITERBI DECODER
10/8 CONVERTER
127A
ADAPTIVE EQUALIZATION CIRCUIT

FIG. 73

PR1 EYE PATTERN

VOLTAGE

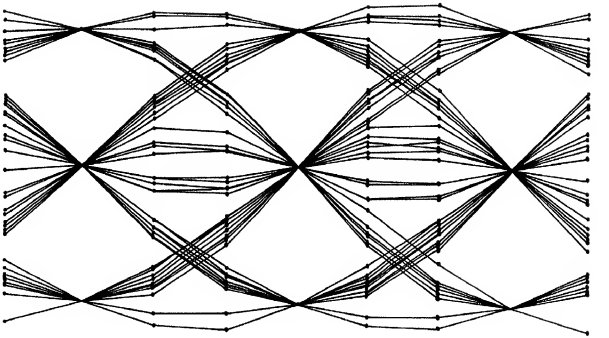


TIME

FIG. 74

PR1 EYE PATTERN

VOLTAGE

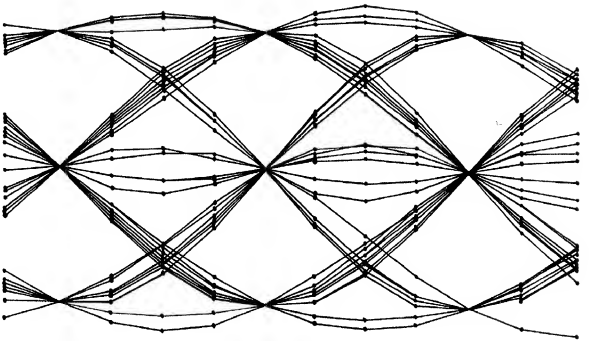


TIME

FIG. 75

PR1 EYE PATTERN

VOLTAGE

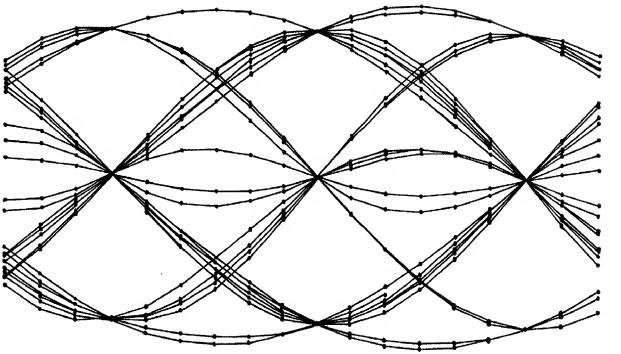


TIME

FIG. 76

PR1 EYE PATTERN

VOLTAGE



TIME

FIG. 77

PR1 EYE PATTERN